Computer Sciences and Data Systems

Volume 2

NASA

Computer Sciences and Data Systems

Volume 2

NASA

OAST Computer Science/Data Systems Technical Symposium

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INTRODUCTION

The Computer Sciences and Data Systems Technical Symposium was held to respond to the communications challenges posed by the rapidly advancing technical arena surrounding NASA personnel. This was the third meeting in what will be periodic gatherings and was hosted by LaRC. Jerry Creedon, Director for Flight Systems at LaRC, performed the welcoming ceremony, and opening remarks were made by Lee Holcomb, Director of Information Sciences and Human Factors at NASA Headquarters.

The intended purpose of these symposia is to bring NASA people together to present their progress, to air their thinking and, in general, to discuss the nature and results of their work within the agency on a wholly technical level. These meetings are not intended as a forum for program reviews, budget presentations or advocacy hearings. NASA personnel have long been recognized as prolific contributors to the journals of technical societies and organizations within the aerospace community. Meetings such as this, organized to improve the interchange of technical information and understanding within NASA, have resulted in valuable connections. These meetings will be continued to be held at approximately 18 month intervals. The Proceedings of the November 1986 Computer Sciences and Data Systems Technical Symposium are presented to provide continuity from one meeting to the next, and to serve as a technical blueprint regarding expected content.

OPTICAL ARCHIVAL DATA STORAGE SYSTEM

COMPUTER SCIENCE/DATA SYSTEMS
TECHNICAL SYMPOSIUM
DOUG THOMAS
MSFC

OBJECTIVE

DEVELOP AND DEMONSTRATE THE TECHNOLOGY REQUIRED TO ARCHIVE LARGE VOLUMES OF MULTI SOURCE MISSION INDEPENDENT DATA SETS AT RATES UP TO 50M BITS/SECOND, GENERATE A COMPREHENSIVE DIRECTORY OF ALL DATA AVAILABLE TO ON-LINE USERS IN NEAR REAL TIME.

DATA BASE MANAGEMENT SYSTEM/MASS MEMORY ASSEMBLY
(DBMS/MMA)

SPACE PHYSICS ANALYSIS NETWORK
(SPAN)
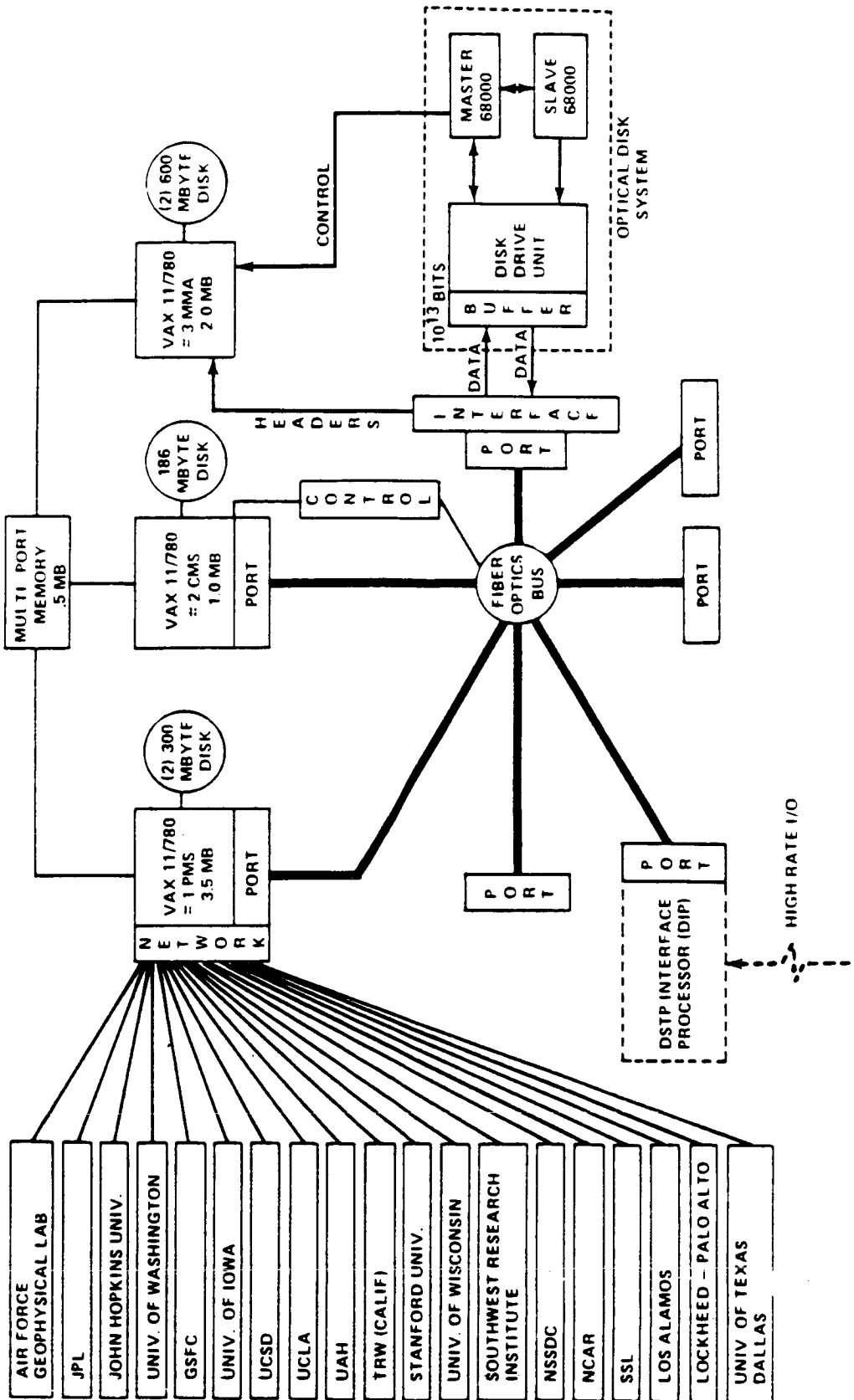
KEY SYSTEM ELEMENTS

- AUTONOMOUS DATA PACKET

- MISSION AND SENSOR INDEPENDENT

- 16—PORT FIBER OPTIC DATA BUS

- BY—PASS CONVENTIONAL COMPUTER I/O TO ACHIEVE HIGH DATA RATES

- OPTICAL DISK RECORDER

- USE OF ARGON LASER TO ACHIEVE HIGH DENSITY RECORDING AND AN AUTOMATED "JUKEBOX" TO PROVIDE A LARGE ONLINE ARCHIVE.

- ORACLE DATA BASE MANAGEMENT SYSTEM

- GENERATE DIRECTORY

- USER QUERY INTERFACE

PACKET FORMAT

PACKET HEADER KEYS

FIELD	PL	DT	MID	SID	SSC	TIME	SUBSEC	USER	DATA
# BITS	32	8	16	16	16	32	32	104	

NOT DEFINABLE
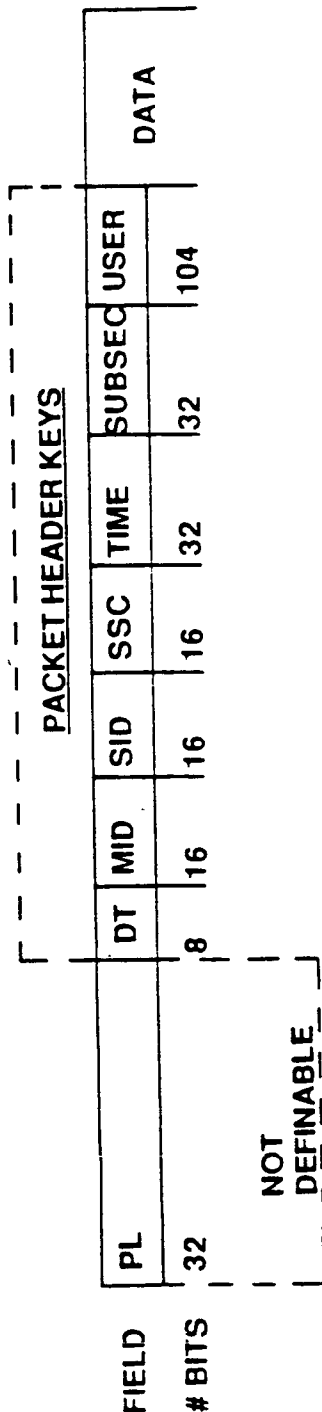
THE FOLLOWING FIELDS ARE COMMON TO ALL PACKETS AND CANNOT BE REDEFINED FOR SPECIFIC APPLICATIONS.

PL   PACKET LENGTH IS THE NUMBER OF BYTES (8-BIT) IN THE PACKET, INCLUDING THE HEADER. THE PACKET SIZE WILL BE A MULTIPLE OF 256 BYTES. THE MINIMUM SIZE FOR A PACKET IS 2 BLOCKS, OR 512 BYTES. THE MAXIMUM SIZE IS:

BLOCKS	BYTES	BITS
1,536	393,216	3,145,728

DT   DATA TYPE IS AN UNSIGNED 8-BIT INTEGER ASSIGNED TO EACH UNIQUE ARCHIVE APPLICATION BY THE DSTP DATABASE ADMINISTRATOR

FIBER OPTIC BUS

- 16 PORT PASSIVE STAR COUPLER

- 50 MICRON CORE GRADED INDEX FIBER

- 100M BITS/SECOND TRANSMISSION

- MANCHESTER CODE USED FOR TRANSMISSION

- TIME DIVISION MULTIPLEXING USING A MASTER CONTROLLER

- TRANSMITTER

    - AlGaAs LED - MOTOROLA MFOE 1200

    - 820 NM WAVELENGTH

- RECEIVER

    - PIN PHOTO DIODE - MOTOROLA MFOD 1100

        - SENSITIVITY OF - 63 dBm FOR 100 MEGABIT MANCHESTER CODE

DISC DRIVE UNIT

CONTROL PANEL

H CARRIAGE

OPTICS PLATFORM

DISC TURNTABLE & DRIVE

READ/WRITE TRANSLATION STAGE & OPTICS

'X' DRIVE

UP & DOWN ELEVATORS

DISC LOADER

RECORD/PLAY LASER

DOWN ELEVATOR DRIVE

UP ELEVATOR DRIVE

CARTRIDGE STORAGE MODULE

ELECTRONICS & UTILITIES

2-7
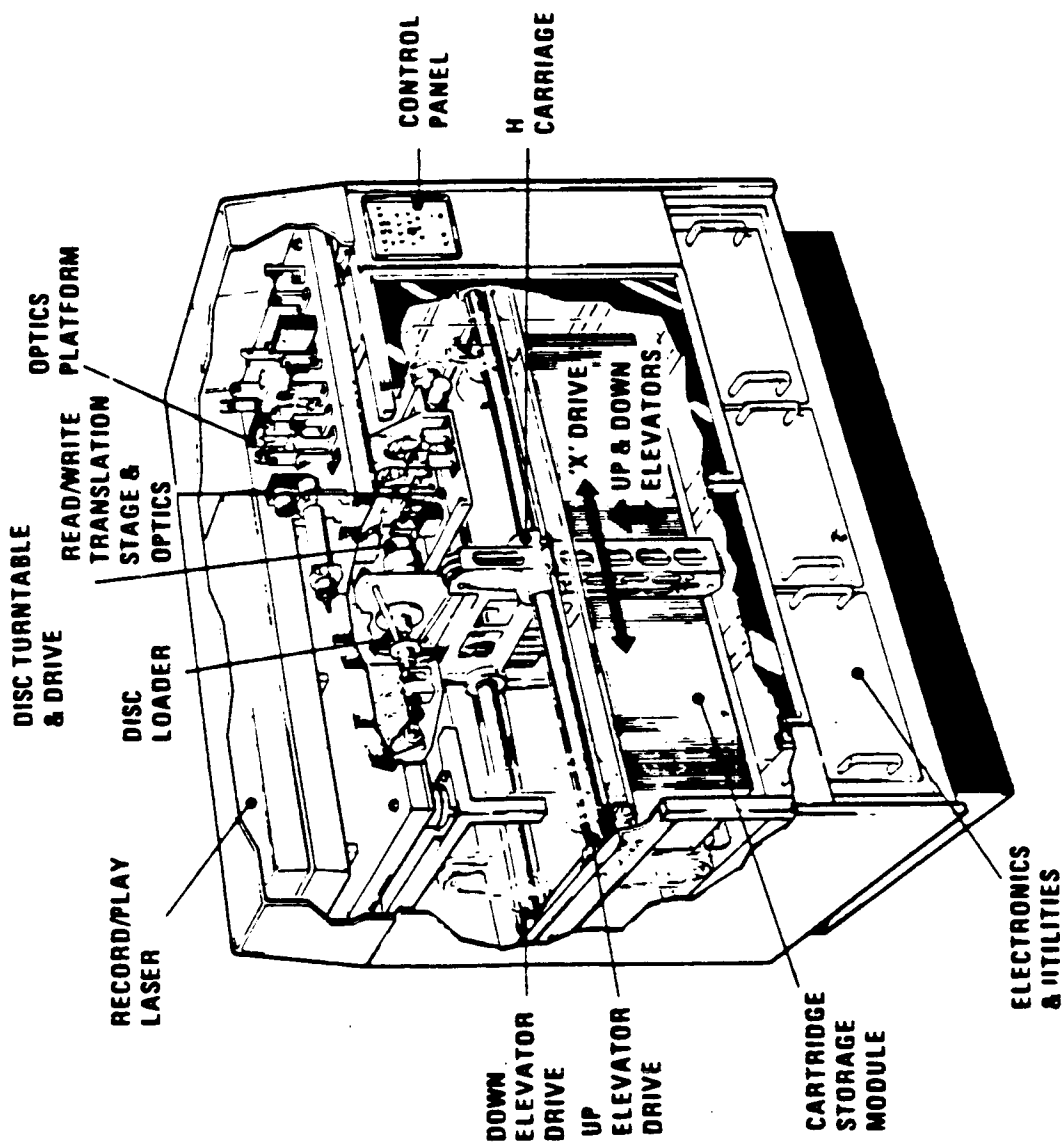
OPTICAL DISK INTERFACE SYSTEM
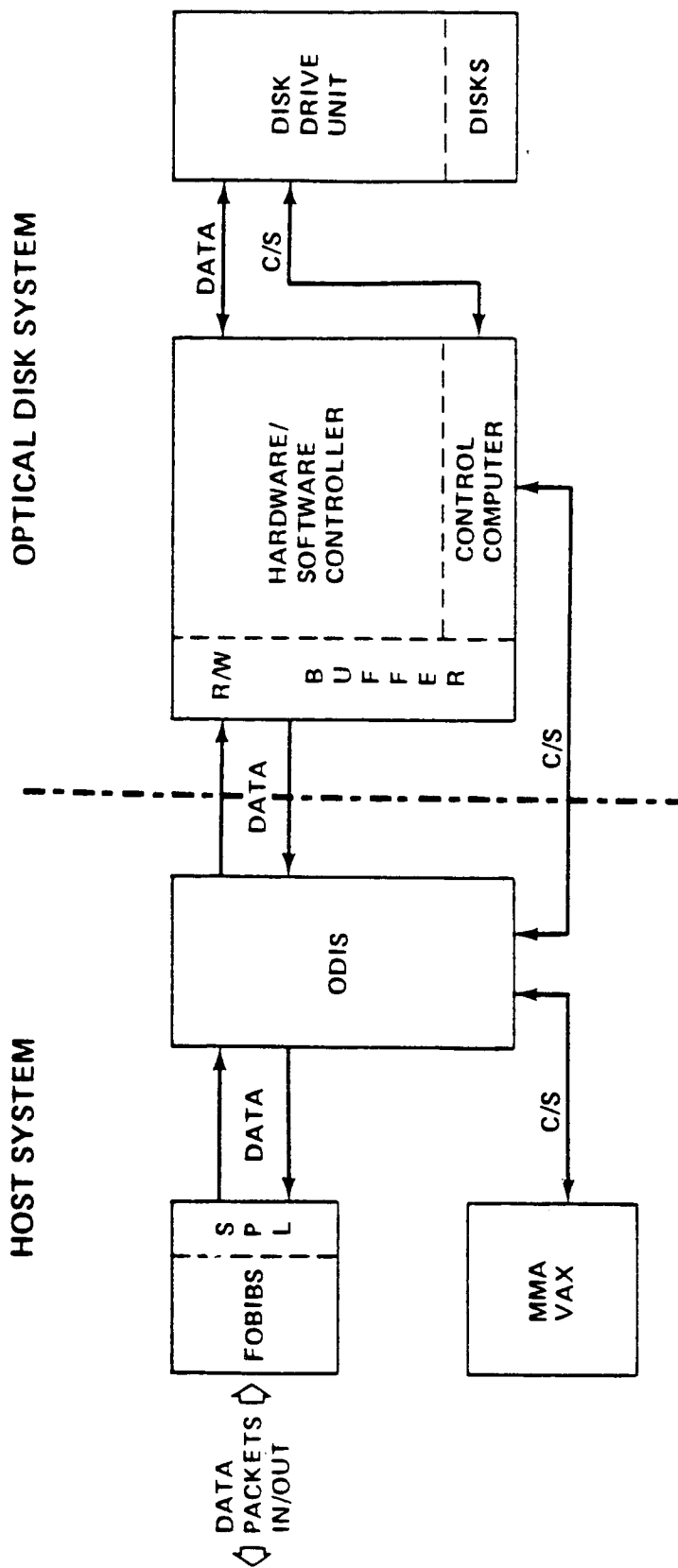
THREE LEVEL ERROR CHECK

- READ—AFTER WRITE FOR RECORDING

  - PERFORMED ON EACH INTERNAL BLOCK (512 BITS)
  - UP TO 40 REWRITES PERMITTED PER TRACK

- 3ϕ7 EDAC FOR OUTSIDE ENVELOP

  - CORRECTS FOR BURST ERROR
  - ENVELOP IS 32K BITS = 1 SECTOR

- 3ϕ7 EDAC FOR INSIDE ENVELOPE

  - CORRECTS FOR RANDOM SINGLE BIT ERRORS
  - ENVELOP IS 512 BITS = 1 BLOCK

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OPTICAL DISK STATISTICS

	DESIGN GOALS	MEASURED DATA	UNITS
ON LINE CAPACITY	10^{13}	$.975 \times 10^{13}$	BITS
ACCESS TIME			
ANY DISK	6.0	6.8	SEC
LOADED DISK	0.5	0.66	SEC
DATA RATES	0–50	0–50	MBPS
BIT ERROR RATE	10^{-8}	10^{-8}	
SPOT SIZE	.5	.5	MICRONS
SPOT SPACING	1.25	1.25	MICRONS
DATA STRUCTURE	TRACK = REVOLUTION	TRACK = REVOLUTION	

● MASTER/SLAVE 68000 BASED CONTROLLER

● 14 INCH ALUMINUM DISK IN PROTECTIVE CARTRIDGE

STORAGE MEDIA COMPARISON

	BITS	MAGNETIC DISK 300M BYTES	MAGNETIC TAPE 6250 BPI	MAGNETIC TAPE 1600 BPI
ONE OPTICAL DISK	7.8×10^{10}	34	66	263
125 OPTICAL DISK	$.975 \times 10^{13}$	4250	8,250	32,875

	OPTICAL DISK	MAGNETIC DISK	6250 BPI MAGNETIC TAPE	1600 BPI MAGNETIC TAPE
ON-LINE HARDWARE FLOOR SPACE (SQ FT)	52	74,800	169,858	673,937
CONTROLLERS REQUIRED		532	1,032	4,110
ON-LINE HARDWARE COST	$2.25M	$106.5M	$206.25M	--
MEDIA COST	187,500	2,571,250	103,125	410,937
STORAGE REQUIRED FOR MEDIA (SQ FT)	52	8,500	796	3,187

POTENTIAL DATA SOURCES FOR ARCHIVE

- SCIENCE DATA

  - SPACELAB EXPERIMENTS

  - PREVIOUS MISSIONS (I.E., DE, ISEE)

  - ANCILLARY

- SPACE SHUTTLE MAIN ENGINE (SSME)

  - TEST FIRINGS

  - FLIGHT DATA

- ENGINEERING DRAWINGS

  - STRUCTURES

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SPACE SHUTTLE MAIN ENGINE NETWORK

NASCOM

SSME DUMP
00 LINK
120 KB

KSC

HOSC DATA
LINK
50 KB

HOSC

PERKIN-ELMER
COMPUTER

MSFC

DSTP
OPTICAL
DISK

PERKIN-ELMER
MSFC
TEST STANDS

PSCN

1.544 MB

1.544 MB

1.544 MB

1.544 MB

PERKIN-ELMER
COMPUTER
NSTL

PERKIN-ELMER
COMPUTER
ROCKETDYNE
CANOGA PARK
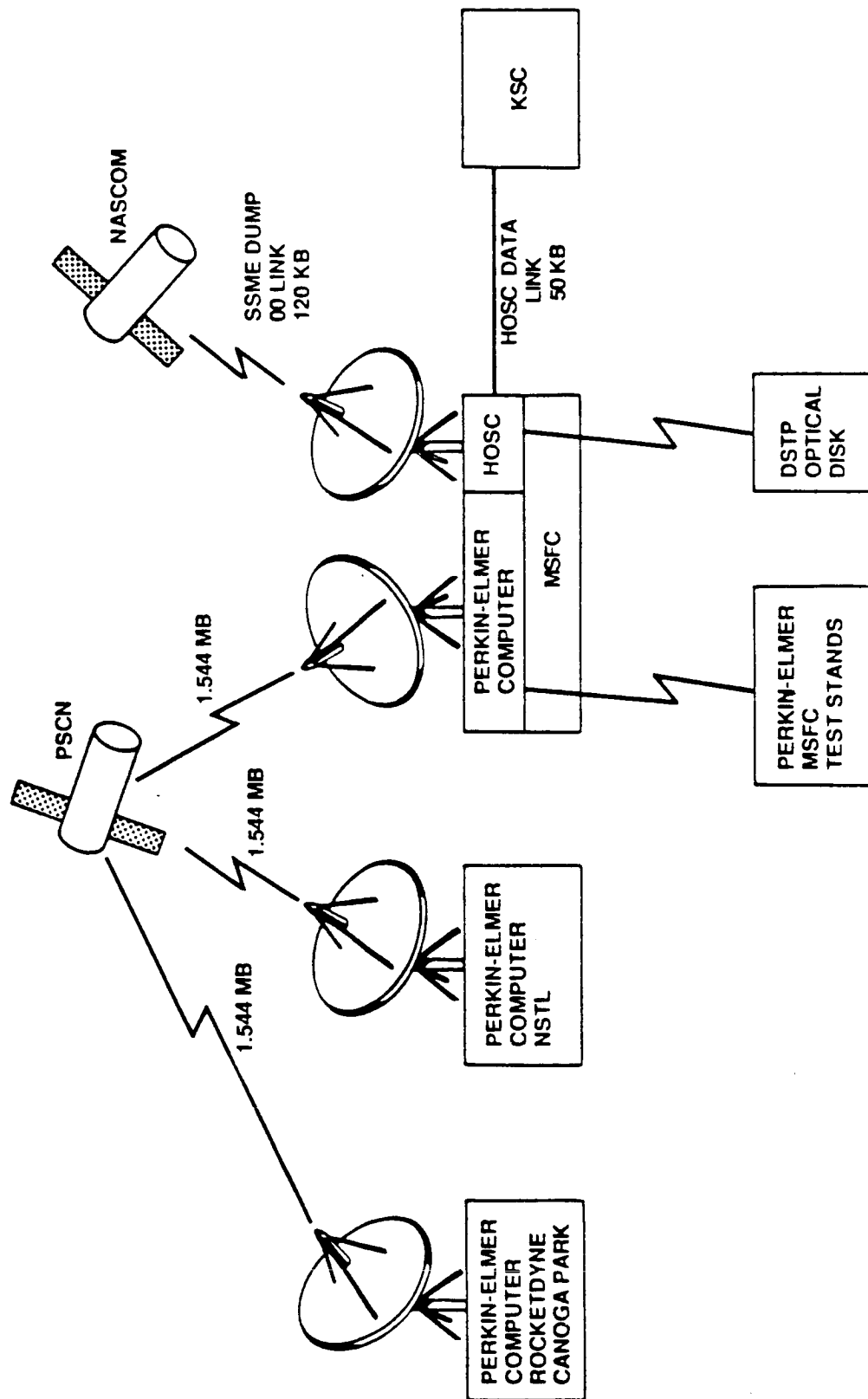
MSFC OBJECTIVES

- INSTALL MULTIPLE TURNTABLES (MINIMUM OF TWO)

  - PROVIDE CONTINUOUS RECORDING

  - USER ACCESS TO PREVIOUSLY RECORDED DATA

- MODIFY SYSTEM TO PROVIDE CAPABILITY TO READ DATA SIMULTANEOUSLY FROM SAME DISK THAT IS BEING RECORDED ON

- REPLACE ARGON LASER WITH LASER DIODE

- MODIFY TO RECORD/READ ERASABLE MEDIA

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FUTURE OPTICAL RECORDING ACTIVITY

IMPROVED LASER DIODES FOR POWER SOURCE

PERFECTING THE ERASABLE MEDIA (MAGNETO OPTICS)

HIGHER RESOLUTION

HIGHER DATA RATES

DEVELOPMENT OF LOW COST HIGH RESOLUTION OPTICAL DISK MEDIA

INFORMATION NETWORK ARCHITECTURES
N. MURRAY/NASA-LARC

OBJECTIVE

RESEARCH AND DEVELOP INFORMATION NETWORKS TO MEET THE ADVANCED AEROSPACE MISSION NEEDS OF FAULT TOLERANCE, HIGH PERFORMANCE, EVOLVABILITY, ADAPTABILITY, SECURITY, AND EFFICIENCY.

APPROACH

o RESEARCH, EVALUATE, CHARACTERIZE THE ARCHITECTURAL TYPE NETWORKS:

- STATIC CENTRAL CONTROL, FAULT TOLERANT, HIGH PERFORMANCE MESH
- ADAPTIVE DISTRIBUTED CONTROL, FAULT TOLERANT, HIGH PERFORMANCE MESH

LARC
INHOUSE
EMULATION

NASA-LARC-INTEGRATION, EVALUATION, MANAGEMENT
C. S. DRAPER LAB - HARDWARE/SOFTWARE, ADVANCED PROTOCOLS
RTI/NO. CAROLINA UNI. - ANALYTIC MODELING
UNI. OF ILLINOIS - ADVANCED PROTOCOLS, THEORETICS

o RESEARCH AND DEVELOP AN ADAPTIVE OPTIC NODE:

HONEYWELL - ANALYSIS, DESIGN

INFORMATION NETWORK ARCHITECTURES

506-58-13/N. MURRAY

● INTEGRATED – DATA, VOICE, VIDEO

● KEY ISSUES OF NETWORKS

  – INFORMATION FLOW/OPERATING SYSTEM (SEPARATE DATA, CONTROL COMMUNICATIONS)

  – SELF-CORRECTING AND REPAIRING/FAULT TOLERANCE (MESH TOPOLOGY)

  – HIGH PERFORMANCE (FIBER OPTICS/INTEGRATED OPTICS, MESH TOPOLOGY)

INFORMATION FLOW BETWEEN COMPUTERS AND OTHER DEVICES REQUIRES A SYSTEM AND ARCHITECTURAL
SOLUTION THAT AFFECTS BOTH HARDWARE AND SOFTWARE. CURRENT SYSTEMS USE EXTENSIVE SOFTWARE
FOR THE INFORMATION FLOW RESULTING IN A SOFTWARE BOTTLENECK; CONTROL ALGORITHMS AND
METHODS FOR TIGHTLY COUPLED, HIGH PERFORMANCE, DISTRIBUTED PROCESSING ARE INADEQUATE; SELF
CORRECTING AND REPAIRING TECHNIQUES ARE NOT BEING FULLY APPLIED TO TODAY'S SYSTEMS.
REAL-TIME, FULL MOTION, DIGITAL COLOR VIDEO REQUIRES DATA RATES IN EXCESS OF 100 MBPS.

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NETWORK ARCHITECTURE/TOPOLOGY

WDM
OPTICAL BUSES

OPTICAL NODE

SERIAL ELECTRONIC INTERFACE

VOICE TRANSCEIVERS

BYTE WIDE ELECTRONIC INTERFACE

COMPUTERS TERMINALS SENSORS

OPTICAL INTERFACE

VIDEO CAMERAS DISPLAYS
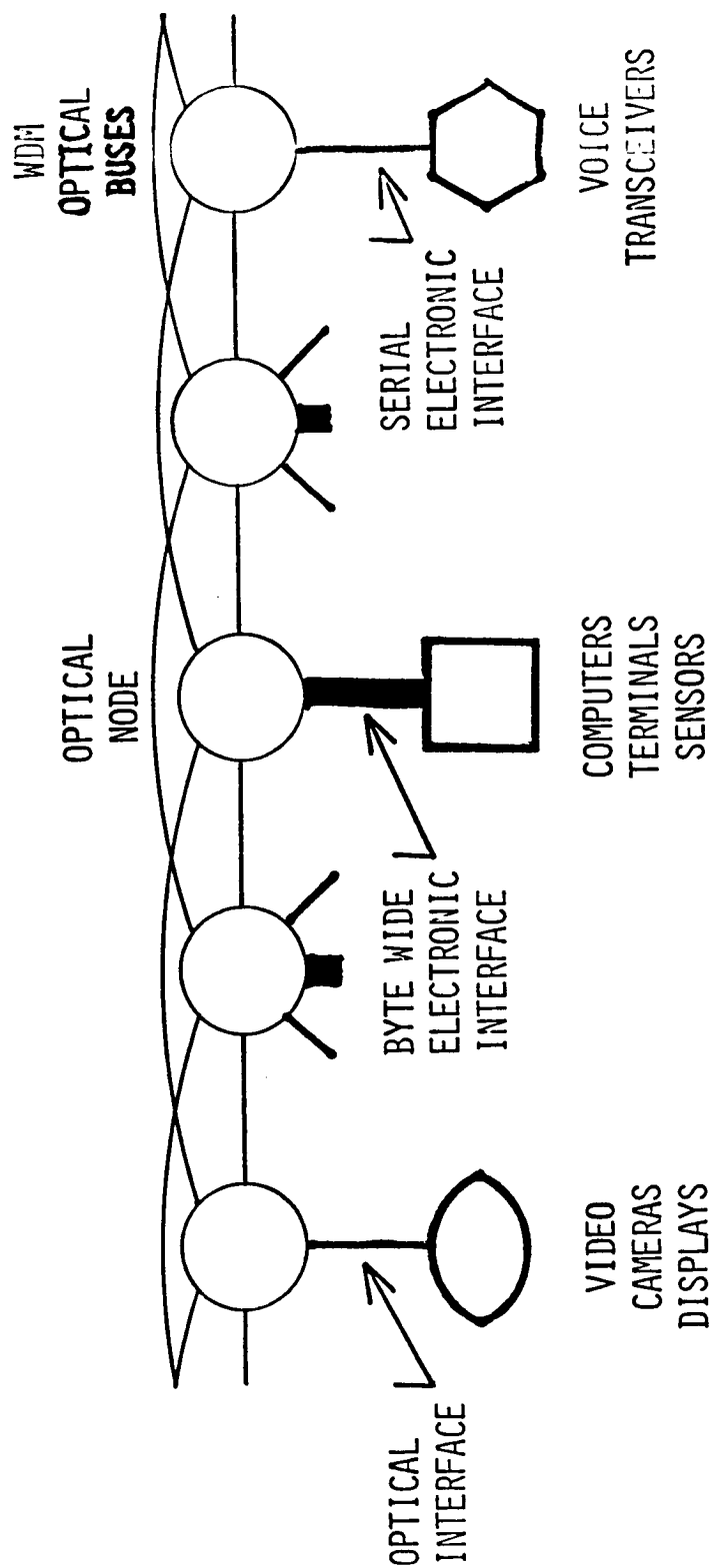
o HIGH PERFORMANCE o

o FAULT TOLERANT o

ELECTRONIC EMULATION OF OPTIC NETWORK

NODE — NETWORK USER COMPUTER

N — NUC
N — NUC
N — NUC
N — NUC
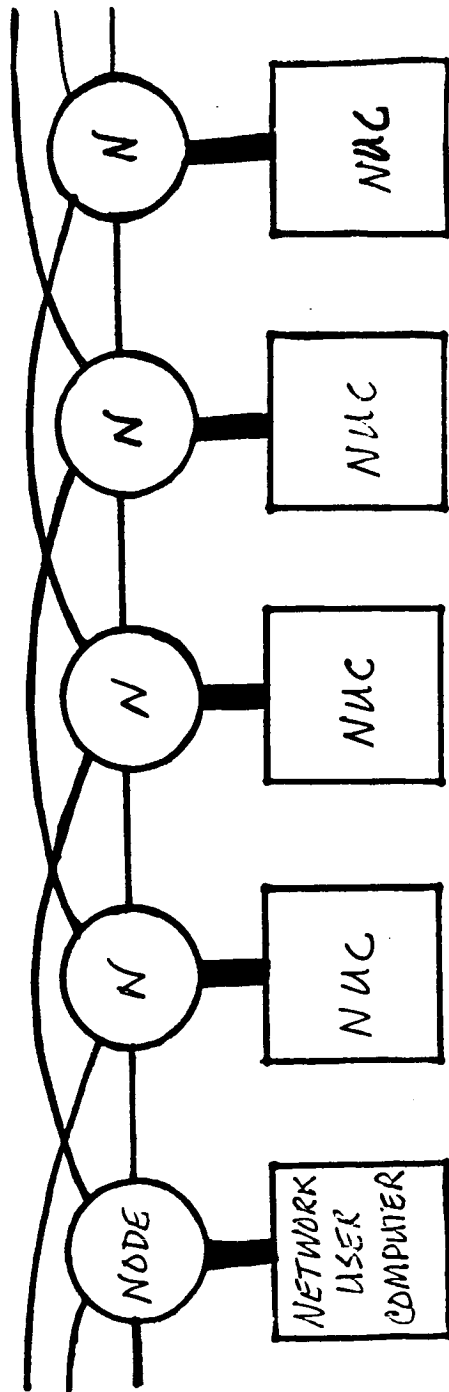
DATA ACCUMULATION
• EVENTS
• TIME
⇓
STATISTICAL
EVALUATIONS

USER SERVICE DEMAND
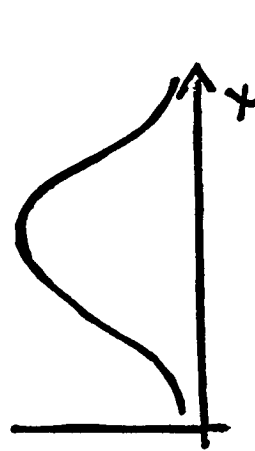
USER SERVICE TIME
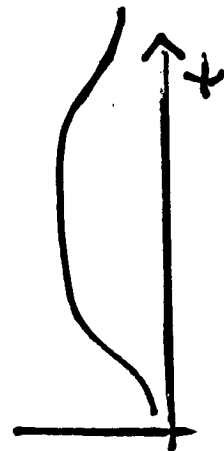
PARAMETRICALLY CONTROLED DISTRIBUTIONS

EVALUATION OF:
• FAILURE DETECT/RECOVER
• CENTRALIZED ROUTING
• DISTRIBUTED ROUTING
• FLOW CONTROL
• NETWORK UTILIZATION
• PEAK LOADING
• NUC/NODE INTERFACES

ROUTING ALGORITHMS

1) NON-ADAPTIVE

   - NO ATTEMPT TO ADJUST TO CHANGING NET CONDITIONS
   - FIXED OR RANDOM ROUTING

2) CENTRALIZED ADAPTIVE

   - CENTRAL AUTHORITY DICTATES ROUTING DECISIONS
   - MORE NEAR OPTIMAL ROUTING
   - ROUTING CONTROL CENTER CAN REPRESENT PERFORMANCE BOTTLENECK

3) ISOLATED ADAPTIVE

   - INDEPENDENT OPERATION
   - ADAPTABILITY VIA EXCLUSIVE USE OF LOCAL NODE DATA

4) DISTRIBUTED ADAPTIVE

   - UTILIZE INTERNODE COOPERATION
   - NODES EXCHANGE INFORMATION TO ARRIVE AT ROUTING DECISIONS

-MCQUILLAN, BBN

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HYBRID FDIR
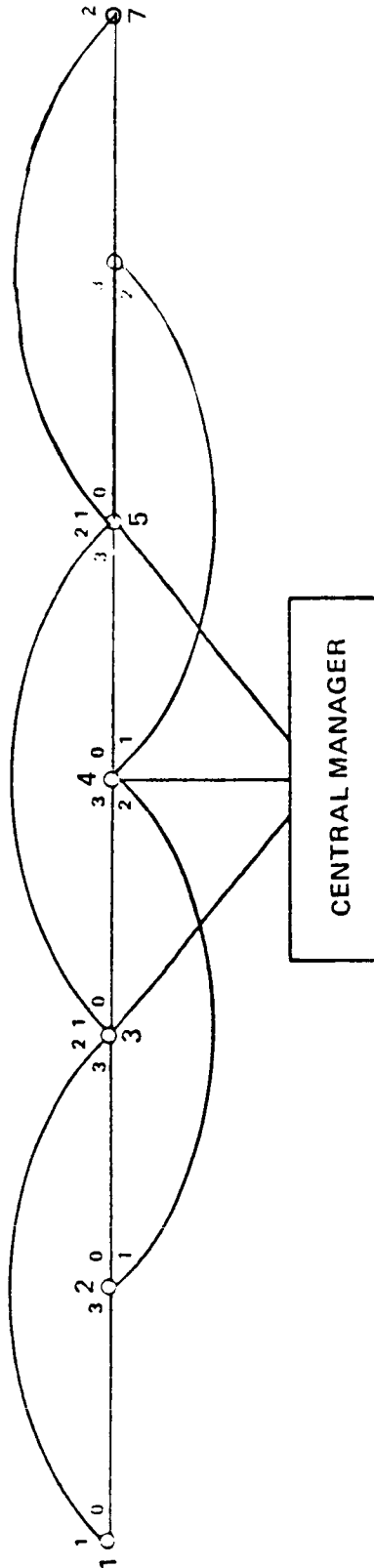
PATH SEARCH ALGORITHM

Purpose

1. Routing data through a meshed network

2. Establishing a circuit set up

3. Adaptive to topological changes

4. Simultaneous communication desirable

EX 1: NORMAL OPERATION
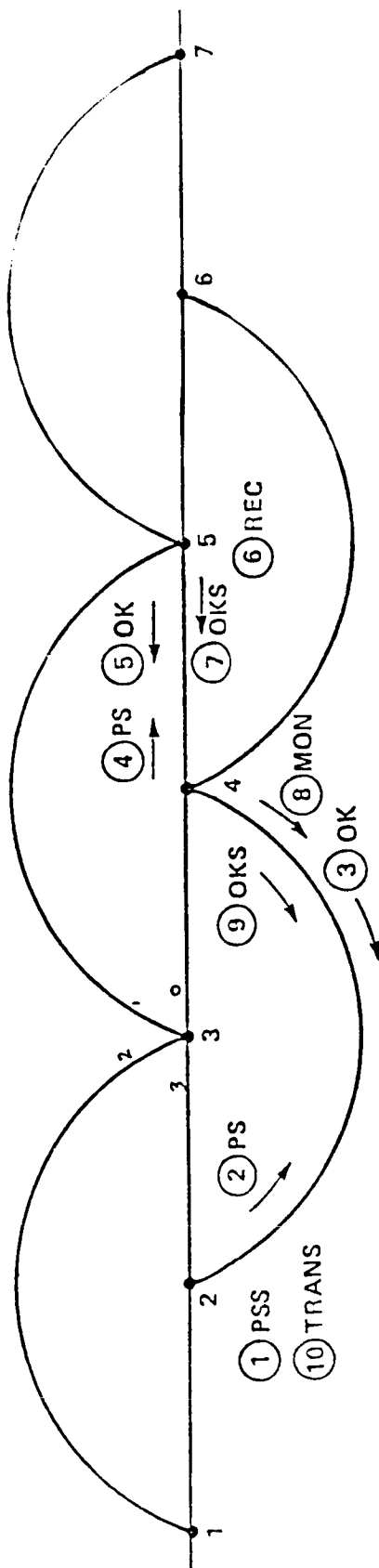
HYBRID APPROACH TO FDIR

o FAULT DETECTION

- BY NODES DURING PATH SEARCH AND DATA TRANSFER

o FAULT COLLECTION

- EACH NODE LOGS FAULT INFORMATION RELATIVE TO ITS PERSPECTIVE

- CENTRAL MANAGER PERIODICALLY COLLECTS FAULT REPORTS TO ACHIEVE A GLOBAL PERSPECTIVE

o FAULT IDENTIFICATION

- CENTRAL MANAGER COGNIZANT OF ALL PORT (LINK) AND NODE FAILURE

- NODES AWARE ONLY OF LOCAL PORT FAILURES

o FAULT RECOVERY

- SHORT TERM RESPONSE

DYNAMIC RECONFIGURATION DURING PATH SEARCH TO AVOID FAILED LINKS

- LONG TERM RESPONSE

ROUTING TABLES RECOMPUTED BY THE CENTRAL MANAGER TO OPTIMIZE ROUTING

CENTRAL MANAGER PASSES NEW TABLES TO NODES

o FAULT NOTIFICATION TO OPERATOR

- CENTRAL MANAGER DISPLAYS FAULT INFORMATION DURING NORMAL NET OPERATION

NETWORK EMULATION/PROTOCOL EVALUATION

<u>CURRENT</u>

FOUR (SIX) NODE NETWORK EMULATION OPERATIONAL IN-HOUSE

CENTRALLY CONTROLLED, PATH SEARCH PROTOCOL INSTALLED
AND RUNNING (CSDL FORMULATED)

<u>FUTURE</u>

* COMPLETE EVALUATION OF PATH SEARCH PROTOCOL

* MOD PATH SEARCH PROTOCOL AND EVALUATE

* EXTEND PATH SEARCH PROTOCOL TO FULLY DISTRIBUTED
  AND EVALUATE

* INSTALL FULLY DISTRIBUTED PROTOCOL (U. OF ILLINOIS
  FORMULATED) AND EVALUATE

EXAMPLE HIGH PERFORMANCE NETWORK
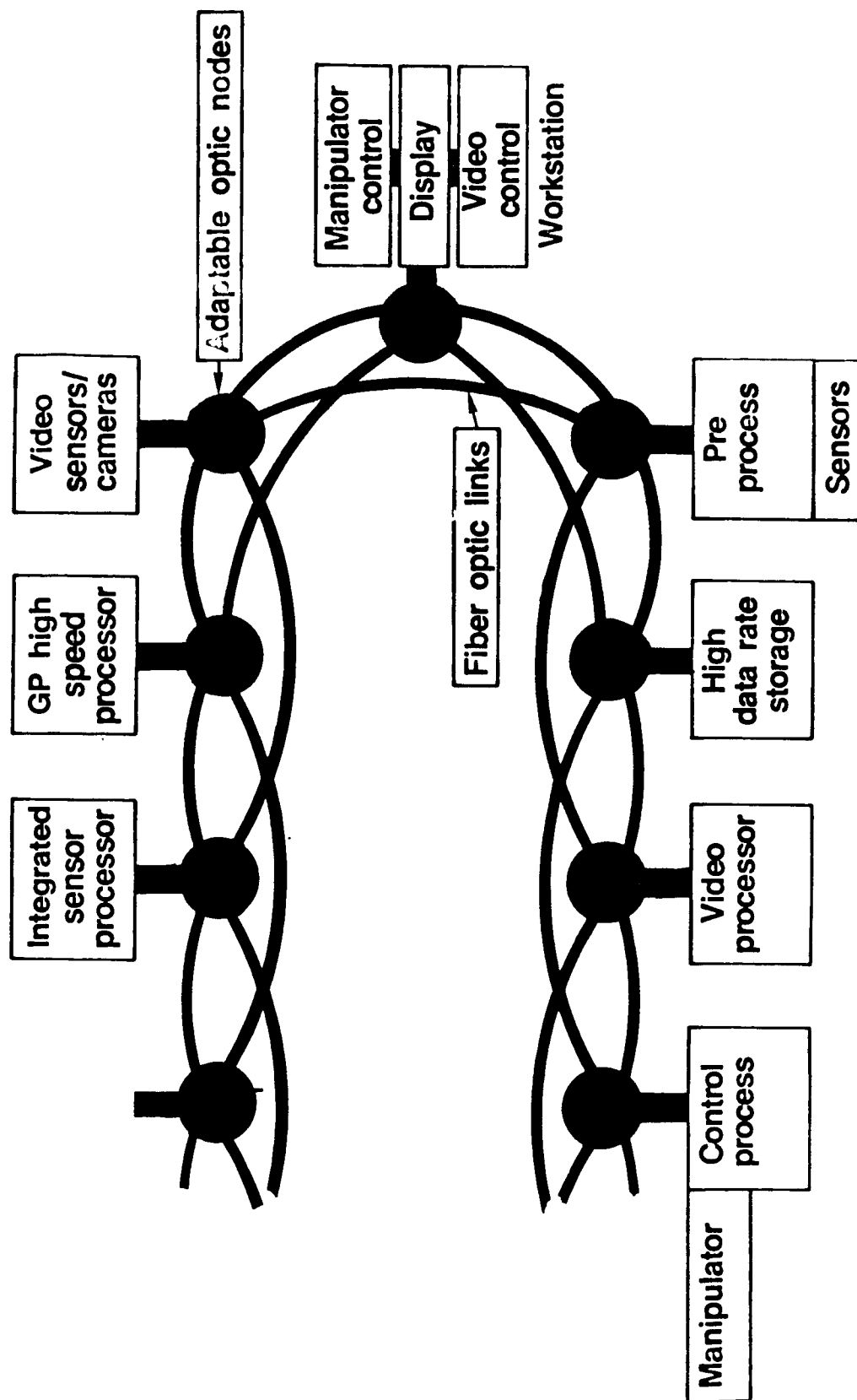
ADAPTIVE OPTIC NODE CONCEPT

Planar
Integrated-Optic
Circuit

Laser
Diode

Optical Fiber
Cable

Optical Fiber
in Etched
Channel

Silicon
Microelectronic
Substrate

Electrical
Lead Outs (Ins)

COUPLES

Fiber
Cable Out

LISTENS

Detector

Optical
Circuit

Miroelectronics

Laser

TALKS

Fiber
Cable In

Peripherals
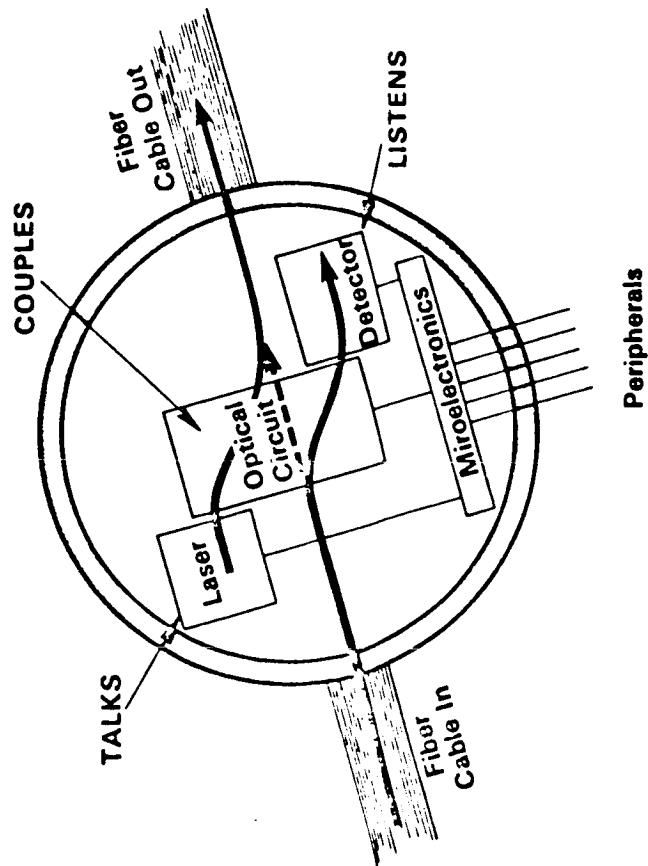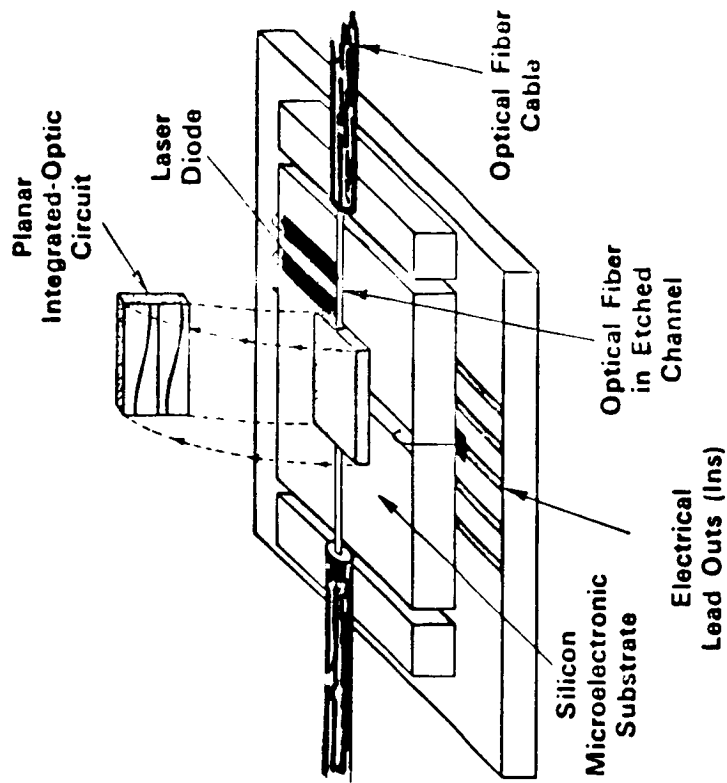
TECHNOLOGY PARTITIONING OF NODE INTERFACE UNIT

2-28
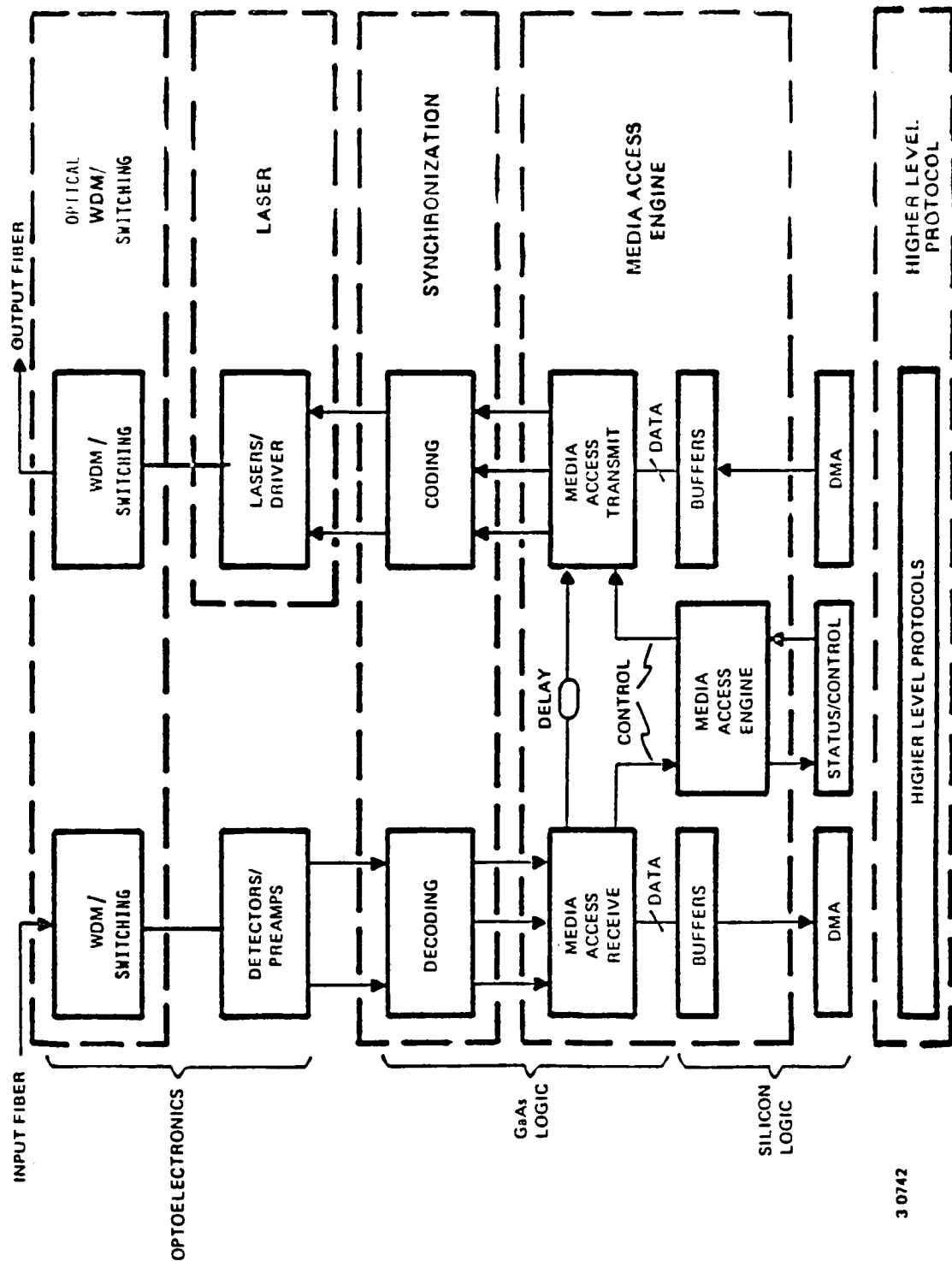
INTELLIGENT OPTIC NODE TECHNOLOGY TIMELINE

TIME / FUNCTIONS	NEAR TERM (1-2 YEARS)	MEDIUM TERM (3-5 YEARS)	LONG TERM (5-10 YEARS)
● E/O	GaAlAs (discrete)	GaAlAs with drive/ detector electronics	Monolithic GaAs
● O/E	Si		
● Fiber	Single mode, non-polarization preserving		polarization preserving?
● Taps, Delay	Fiber	SAW	TBD
● Amplification	Si	GaAs	Monolithic GaAs
● Switching	LiNbO3 (bulk)	LiNbO3 / ZnO ?	ZnO? / AlGaAs
● Synchronization	Si / GaAs	GaAs (discrete)	Monolithic GaAs
● Frame/Address Recognition	Fiber / GaAs	SAW / GaAs	TBD
● Conflict Resolution	Si / GaAs	GaAs	Monolithic GaAs
● Routing	N/A	Si / GaAs (discrete)	
● Higher Level Protocols		Si	

ADAPTIVE OPTIC NODE

INITIAL DEFINITION OF A HIGH PERFORMANCE NETWORK
USED FOR NODAL REQUIREMENTS

INITIAL FUNCTION DEFINITION OF OPTIC, INTEGRATED
NODE AND TECHNOLOGY TIMELINE

CONDUCTING RE-ASSESSMENT OF NETWORK AND NODAL
DEFINITIONS

o MORE GENERAL MISSION SCENARIO

o WELL SUITED FOR OPTICS, INTEGRATED OPTICS

NASA OAST VHSIC Technology

Review for Computer Science Symposium

H. F. Benz

VHSIC Liaison

(804) 865-3777

This Program is an aggressive system
level insertion program for VHSIC technology
capture from DoD / OUSDRE and insertion into
NASA Aerospace missions.

Topics

NASA – OAST VHSIC Processor Development

Insertion Candidates

Parallel SBIR Developments

Why VHSIC for NASA ?

Testability

   Cost Savings of Remote Testing in Ops Environment

   Free Flyers, Shuttle, Space Station

   VHSIC has Built In Test to Chip Level

Maintainability

   System Cost Savings of Common Tools, Software,

   Line Replaceable Modules

Upgradeability

   Hardware / Software Upgradable with Technology

   Transparency through Functional Description

   and Partitioning in CAD / CAM Environment

Availability

   20 Year Technology Life with Multiple Suppliers

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NASA – OAST – VHSIC – SDIO

Processor Development

Team:

NASA LaRC, Benz, Hayes, Looney, Nichols, Gerdes, Andrews

OUSDR&E VHSIC P.O., Maynard

AFWAL, Hines, Garcher

AFSTC, Herndon

USA MICOM, Sproat

Westinghouse, Vyrostek

RTI, Clary

SRI

NASA JSC / C. S. Draper Labs., Chevers

Spacebourne Inc., Timoc

VHSIC PROCESSOR TECHNOLOGY DEVELOPMENT

OBJECTIVE

o To conduct studies which facilitate insertion
of VHSIC technology into advanced embeddable
applications

- Space Station
- EOS
- Aerospace transportation systems
- Experiments

APPROACH

o Codevelop processor technology base
o Demonstrate simplex and triplex algorithms
  in VHSIC system architecture
o Focus toward test bed demonstrations
o Develop in-house experience with 1750A ISA
o Supportive task assignment studies
o Monitor VHSIC Phase 2

NASA VHSIC INSERTION PROGRAM

Significant FY86 Accomplishments

- Operating Fairchild 1750A
- Operating SEAFAC—validated Westinghouse 1750A
- ADAS installed in-house
- Developed models of Fairchild and TI 1750As
  - supplied to Air Force contractors
- Procurement initiated for multiprocessor demo.

Expected FY87 Accomplishments

- Comparative characterization of TI VHSIC 1750A brassboard
- Simulate optimized performance of triplex algorithm on AFWAL multiprocessor
- Define task assignment approach

CURRENT MULTIPROCESSOR THRUST

Demonstrate 4-processor multiprocessor system configuration with asynchronous, concurrent processing of both simplex and triplex algorithms.

- AFWAL system modules
- Self-testing and fault logging
- Ada application software
- Autonomous detection of processor failures and system reconfiguration

VHSIC TECHNOLOGY INSERTION

RADIO RECEIVER/ANTENNA

IMAGING RADAR

IMAGING SPECTROMETER

IMAGER

SPECTROMETER

NO. OF EOS INSTRUMENTS

4   8   12   16
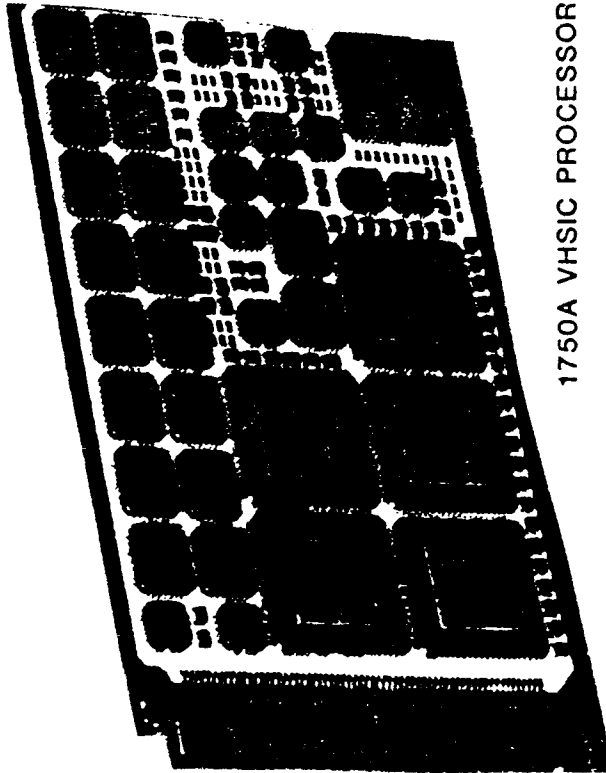
1750A VHSIC PROCESSOR

BENEFITS

o   MULTIPLE 1750A PROCESSOR DEVELOMENTS

o   HIGH SPEED

o   FAULT TOLERANT

o   ADA LANGUAGE

o   SIZE,WEIGHT,POWER,RELIABILITY
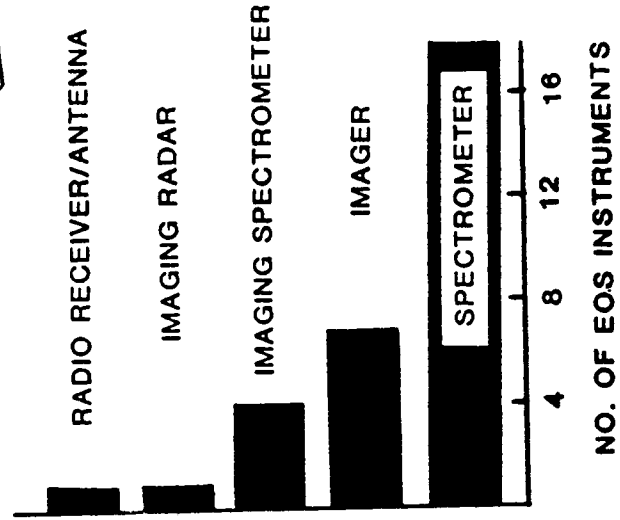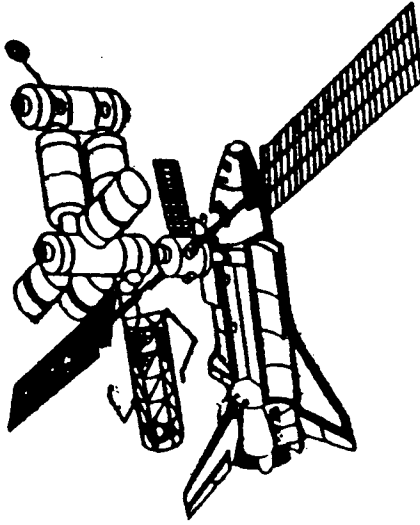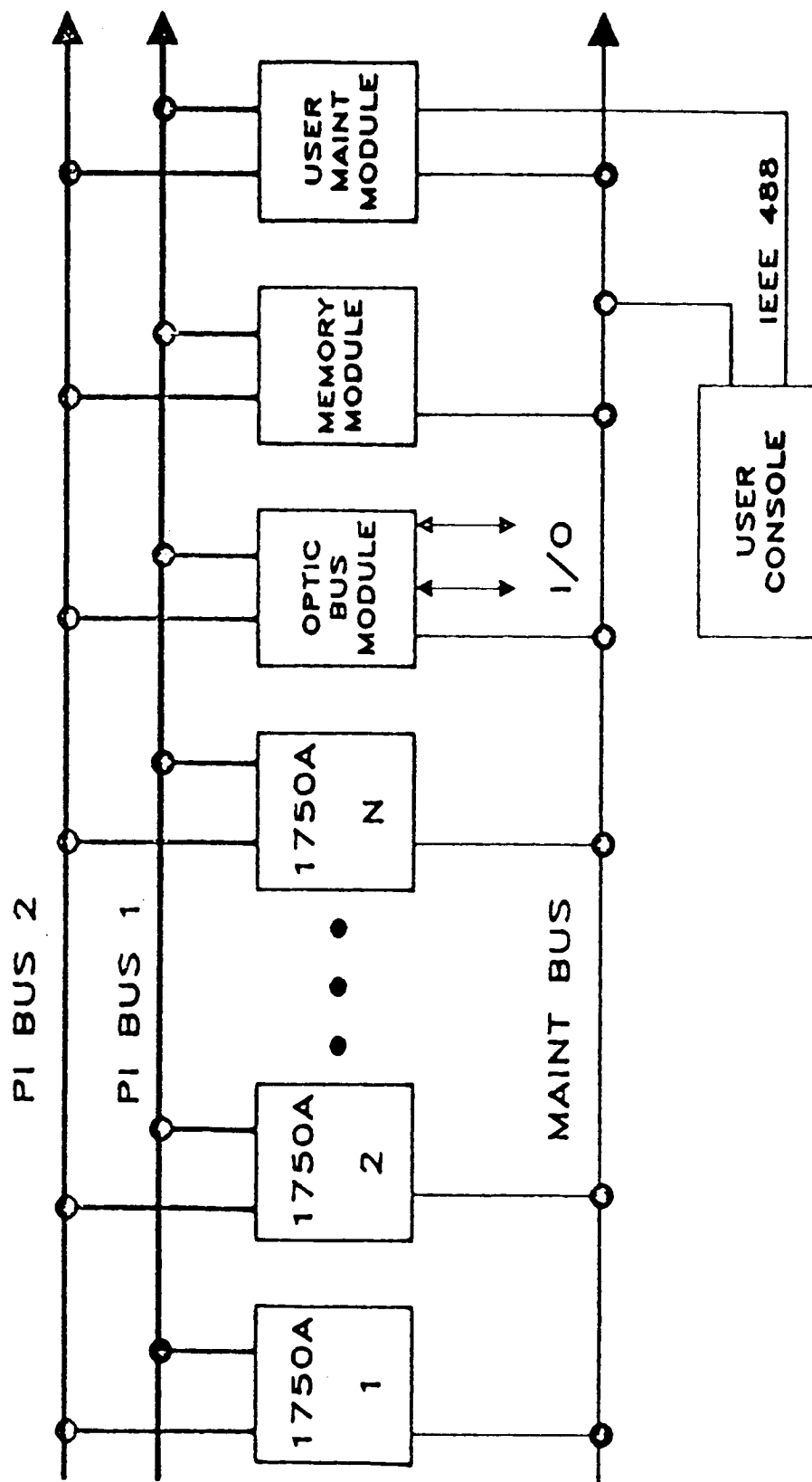
Figure 1. Block diagram of 1750A parallel processor system.

Advanced Autopilot Algorithm Directed Graph
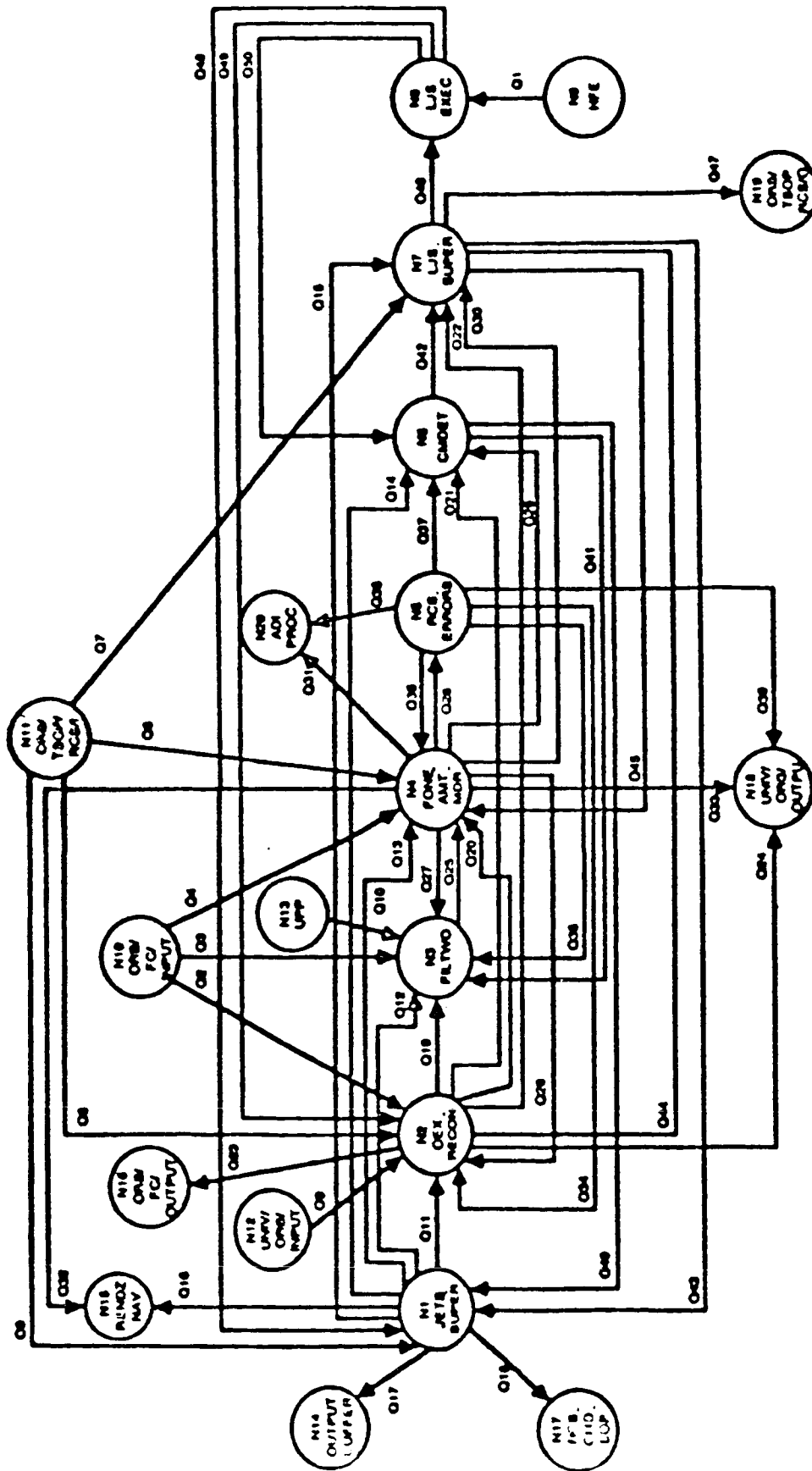
Elements

Systems and Schedules

Hardware

Software

Operating Systems

System Development Tools

Systems and Schedules

EOS

NSSD

SS DMS

System Development

VHSIC II
Superchips

V1750A
Space

V1750A
Avionics

V1750A ADM'S

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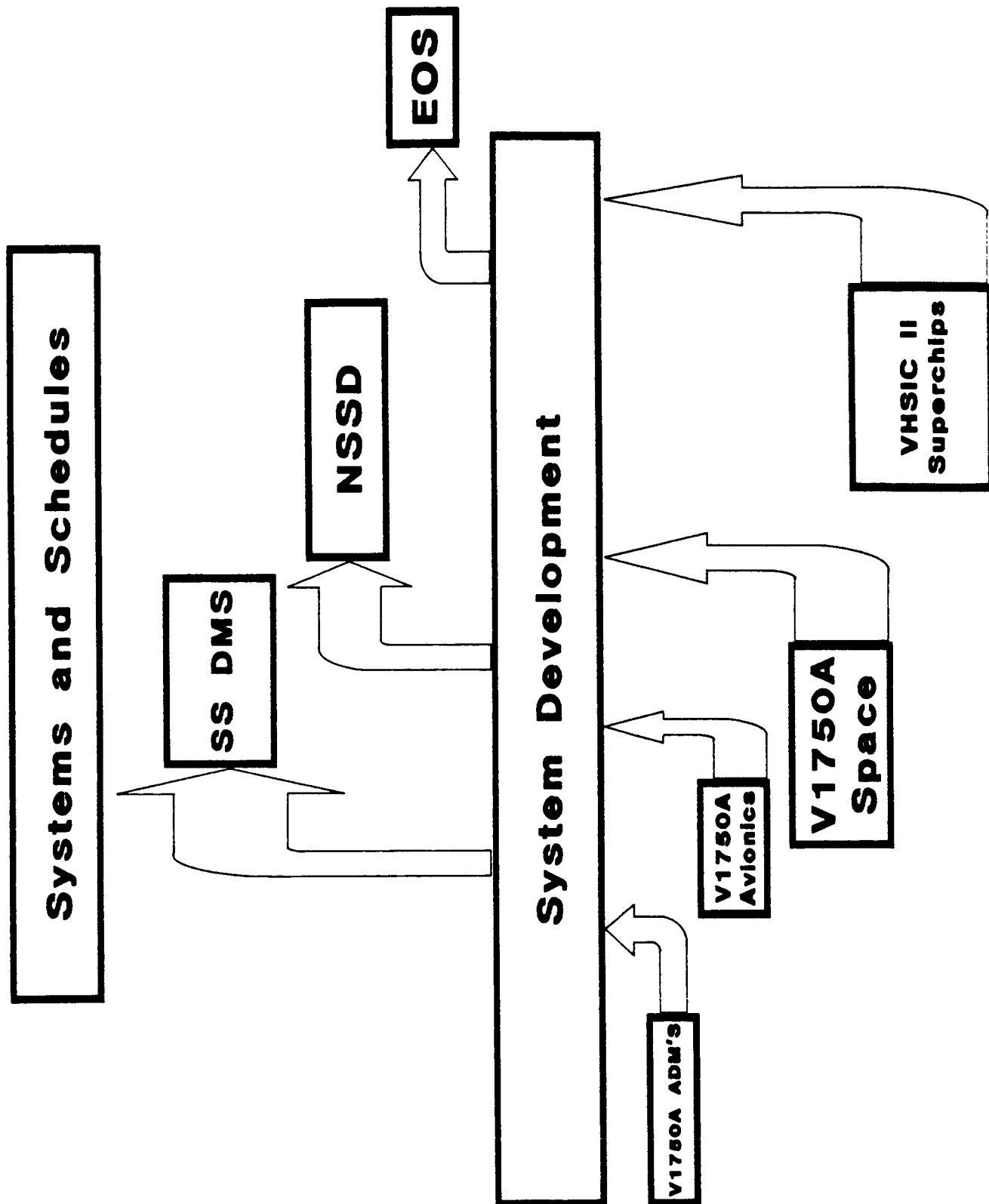
System Hardware Development

VHSIC I

Today

PI Bus

F.O. PI

Available Hardware

F9450

W VP2

TI
V1750A

V1750A'S

VHSIC II
Superchips
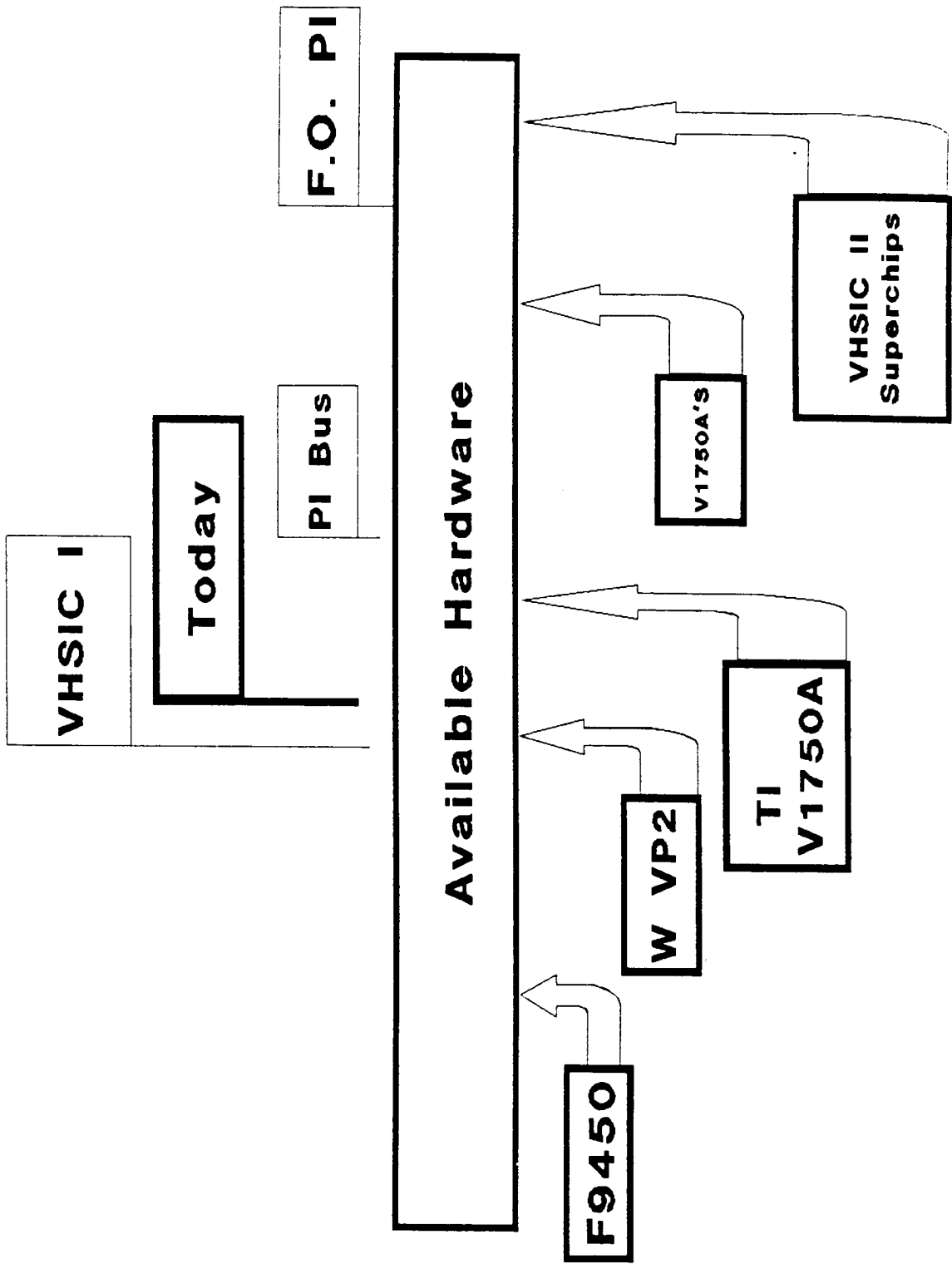
Software Development

Algorithm Development
OEX Autopilot
State Variable
Kalman Filter
Pattern Recognition

Available Software

- 1750 Ass'y
- Jovial
- W – Ada
- DEC Ada
- DEC-Ada 1750A

Data Graph Oriented O / S

Simulation
Theoretics
Findings

Operating System Development

Verdix

W - DGM

RTI - ADAS

ODU
Multibus

SRI/
West
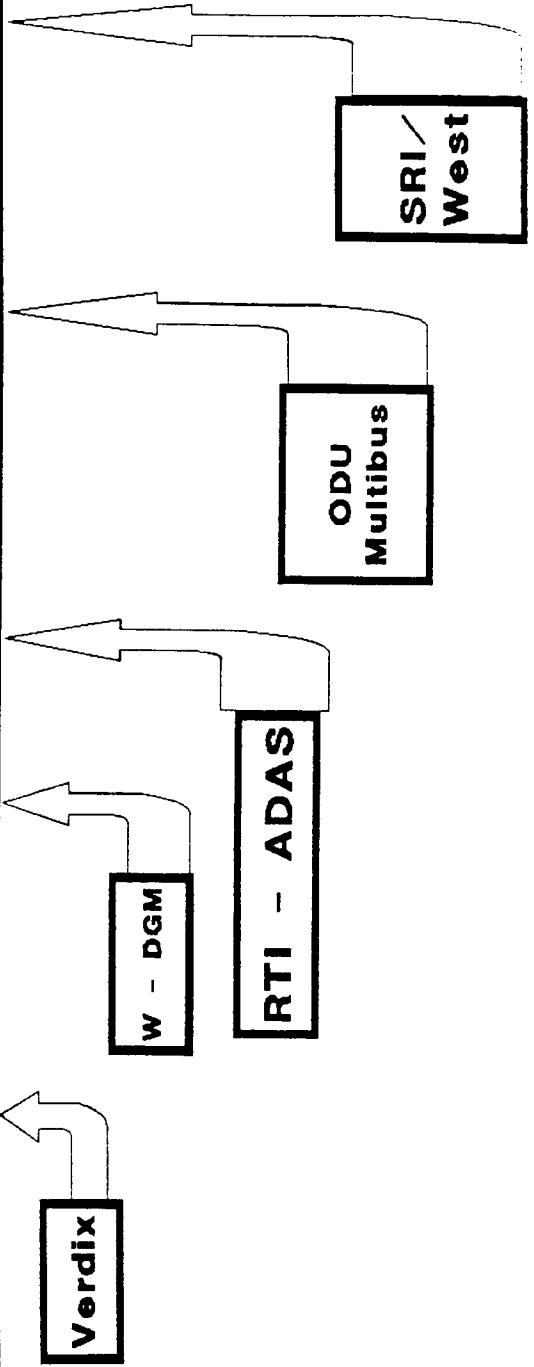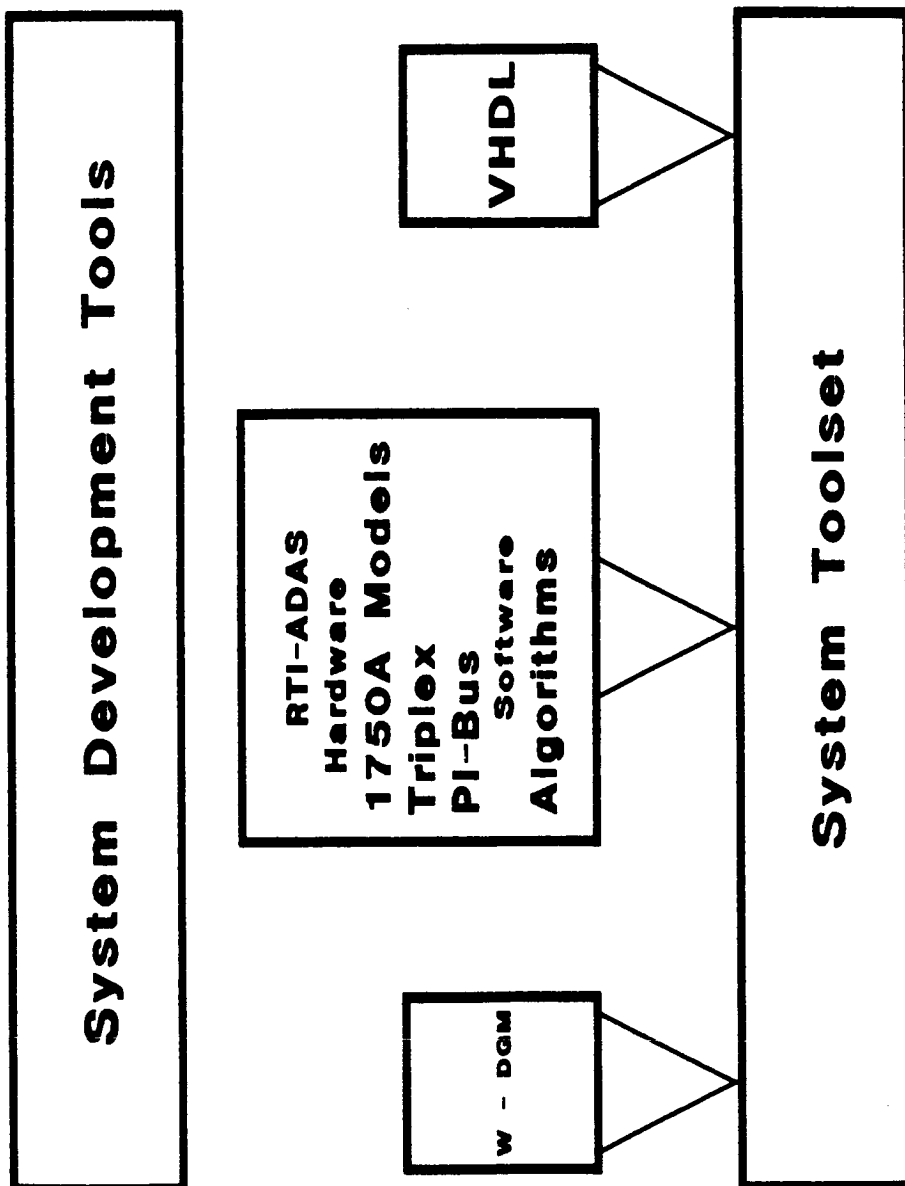
Insertion Candidates Studied

Space Station
- Initial Study / VHSIC-Westinghouse
- Recommended by SS Architecture Contractors
  - MDAC/IBM/Honeywell/Harris

Earth Observing Satellite System
- Mission Set Study Complete

Synthetic Aperature Radar
- Currently Under Study

Related Developments

Fully Self Testable 1750A Chipset

Spacebourne Inc. Small Business Innovative Research Program Design Validating Developmental Breadboard to be delivered 4 / 87.

Experiments

Rationale

Single Event Upset testing and system recovery and system revalidation after known upsets in the complete benign space radiation environment for VHSIC complexity self-testable aerospace systems profoundly affects the system reliability of such systems and is not currently being developed or tested.

Proposals

NASA Space Station Technology Development Mission

NASA-OAST Inreach

Topics

NASA – OAST VHSIC Processor Development

Insertion Candidates

Parallel SBIR Developments

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SEMICONDUCTOR LASER AND FIBER OPTICS TECHNOLOGY

InGaAsP DISTRIBUTED FEEDBACK LASER

AlGaAs CSP LASER FOR ACTS

LINEAR ARRAY FOR OPTICAL DISK BUFFER

PHASED ARRAY LASER FOR OPTICAL COMM

F.O. COMMON MODULE TRANSCEIVER FOR SPACE STATION

WAVELENGTH DIVISION MULTIPLEXING

H D HENDRICKS
NASA LANGLEY

SEMICONDUCTOR LASER TECHNOLOGY

InGaAsP DISTRIBUTED FEEDBACK LASER

OBJECTIVE: DEMONSTRATE HIGH SPEED SEMICONDUCTOR LASERS

APPROACH: DESIGN AND DEVELOP InGaAsP DFB LASERS

JUSTIFICATION: INFORMATION SYSTEMS OPTICAL COMMUNICATIONS

ACCOMPLISHMENTS: 10 MILLIWATTS — 2 GBIT CW AND RT OPERATION

FY 87: MONOLITHIC NARROW LINEWIDTH LASER

RIDGE GUIDE
DISTRIBUTED FEEDBACK LASER
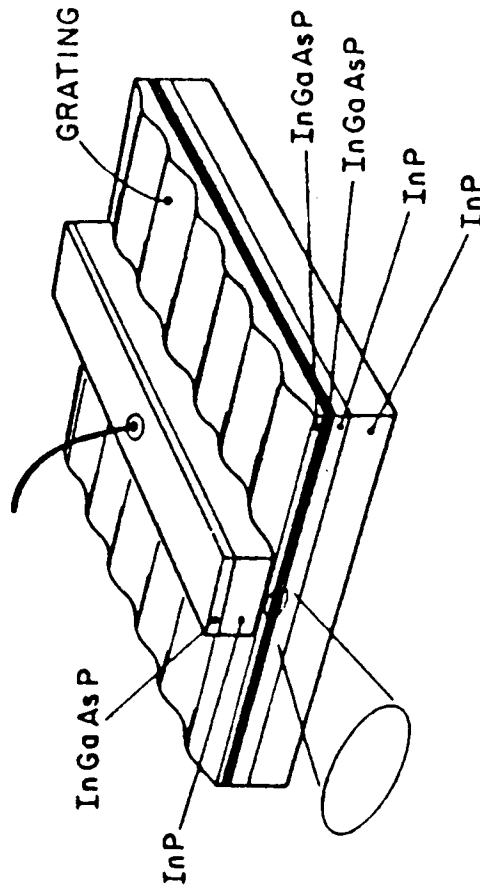
NO MODE HOPPING
REDUCED CHIRPING
2 GHz MODULATION
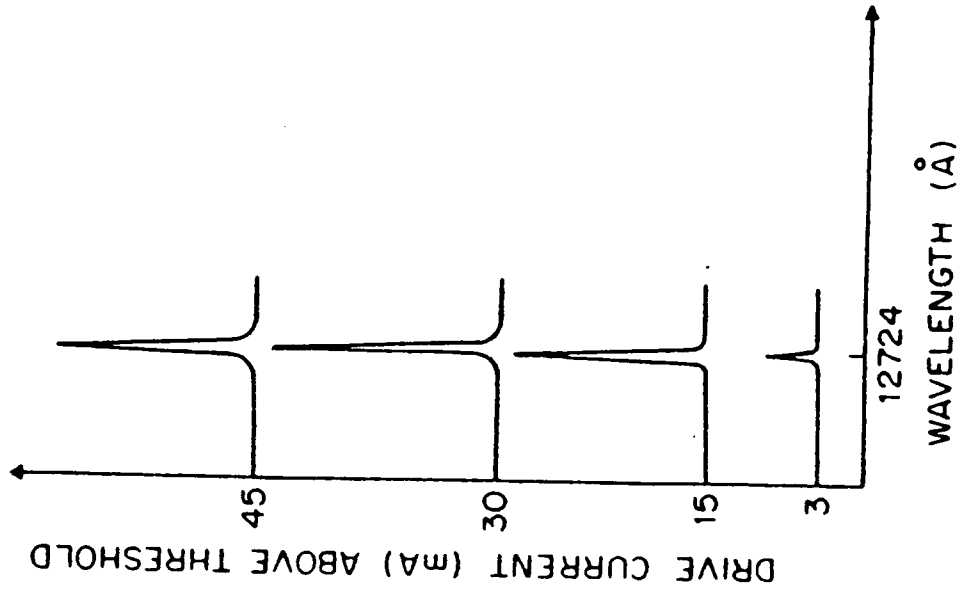
SEMICONDUCTOR LASER TECHNOLOGY

AlGaAs CSP LASER FOR ACTS

OBJECTIVE: HIGH POWER, LONG LIFE 300 MBIT MODULATION

APPROACH: BUILD TECHNOLOGY ON AlGaAs CSP LASER

JUSTIFICATION: HIGH CAPACITY FREE SPACE OPTICAL COMM

ACCOMPLISHMENT: 50/100 MILLIWATTS 300 MBIT MOD. IMPROVED LIFETIME 40 MW DFB LASER

FY87: INCREASE LIFETIME IMPROVE DFB

SEMICONDUCTOR LASER TECHNOLOGY

PHASED ARRAYS FOR OPTICAL COMM.

OBJECTIVE: SINGLE LOBE DIFF. LTD.
0.5-5 WATTS
0.3-4 GBIT MOD.

APPROACH: AlGaAs COUPLED
MODE TECHNOLOGY

JUSTIFICATION: FREE SPACE COMM.
INCREASED B. W.
ANTENNA SIZE <10

ACCOMPLISHMENTS: FOUR ARRAY TYPES
400 MW POWER

FY86: SINGLE LOBE DIFF. LTD.
500 MILIWATTS

SEMICONDUCTOR LASER TECHNOLOGY

LINEAR ARRAY FOR OPTICAL DISK BUFFER

OBJECTIVE: DEMONSTRATE 10 ELEMENT ARRAY

APPROACH: BUILD TECHNOLOGY ON AlGaAs CSP LASER

JUSTIFICATION: TECHNOLOGY FOR 10E12 OPTICAL DISK BUFFER

ACCOMPLISHMENTS: DEMO. 10 ELEMENT ARRAY 30 MILLIWATTS OUTPUT IDENTICAL FAR FIELDS

FY87: INCREASE YIELD DEMONSTRATE LIFETIME

AlGaAs PHASED ARRAY SEMICONDUCTOR LASERS

PROGRESS/STATUS

PHASED ARRAY OF CSP-LOC LASERS

VARIABLE SPACING ARRAY

MODE MIXING ARRAY

SURFACE EMITTERS

"Y" COUPLED ARRAY

AlGaAs PHASED ARRAY SEMICONDUCTOR LASERS

SUMMARY

EVALUATED THREE ARRAY DESIGNS

DEMONSTRATED 400 MILLIWATTS

PROBLEM DOUBLE LOBED BEAM

DESIGNING SURFACE EMITTER
AND "Y" COUPLED ARRAYS

FIBER OPTIC TRANSCEIVER

TRANSMITTER

```
┌───────┐   ┌────────┐   ┌─────────┐   ┌───────┐   ┌────────┐
│ INPUT │───│ DRIVER │───│ CURRENT │───│ LASER │───│  OUT   │
│       │   │        │   │ MIRROR  │   │       │   │  PUT   │
└───────┘   └────────┘   └─────────┘   └───────┘   └────────┘
```

RECEIVER

```
┌───────┐   ┌──────────┐   ┌──────┐   ┌─────────┐   ┌────────┐
│ INPUT │───│ DETECTOR │───│ AGC  │───│  COM-   │───│  LINE  │
│       │   │ PREAMP   │   │ AMP  │   │ PARATOR │   │ DRIVER │
└───────┘   └──────────┘   └──────┘   └─────────┘   └────────┘
```

FIBER OPTICS TECHNOLOGY

F. O. COMMON MODULE TRANSCEIVER

OBJECTIVE: MIL/SPACE QUALIFIED F. O. TRANSCEIVERS

APPROACH: DEVELOP AND DEMO. 10, 50, 200 & 1000 MBIT TRANSCEIVERS

JUSTIFICATION: TRANSCEIVERS FOR F.O. NETWORK ON SPACE STATION

ACCOMPLISHMENTS: EDM FOR 10, 50 & 200 MBIT TX/RX PROTOTYPE 1000 MBIT

FY87: MIL/SPACE QUAL.

FIBER OPTICS TECHNOLOGY

WAVELENGTH DIVISION MULTIPLEXING

OBJECTIVE: DEMONSTRATE WDM TECHNOLOGY

APPROACH: DEVELOP WDM COMPONENTS

JUSTIFICATION: NETWORK EFFICIENCY
INCREASED CAPACITY
FAULT TOLERANCE

ACCOMPLISHMENTS: 4 OPTICAL MUX/DEMUX
500 MBIT TX/RX
WDM INFO SYSTEMS

FY 87 12 CHANNEL DEMUX

High Speed Token Ring Performance Analysis

Marjory J. Johnson

RIACS
NASA Ames Research Center

ABSTRACT

The Fiber Distributed Data Interface (FDDI) is an ANSI draft proposed standard for a 100 megabit per second fiber-optic token ring. We have been studying FDDI because it is a candidate for use on the Space Station. In addition there is widespread interest in the protocol among governmental agencies other than NASA. This paper discusses both analytical and simulation studies of FDDI performance. Fairness of channel access for non-time-critical traffic using the FDDI protocol was studied analytically. Results show that fairness of the protocol depends on the relationship between frame size, the expected token rotation time, and the number of stations on the ring. The simulation study discussed herein was conducted to determine the suitability of FDDI for a specific governmental application.

FDDI token ring

- Fiber Distributed Data Interface

- Draft proposed ANSI standard

- 100 Megabit per second fiber—optic ring

- Timed token protocol

- Two classes of service

  - Synchronous — guaranteed bandwidth

  - Asynchronous — non—time—critical

Potential FDDI Uses

- Space Station

- SAFENET II — navy submarines

- Federal Aviation Authority

- Naval Ocean Systems Center

- National Security Agency

- Northrup — military aircraft

Reasons for Strong
Interest in FDDI

- High speed protocol

- Emerging standard

- FDDI's flexibility to adapt to various applications

- FDDI's ability to integrate voice, video, and data

- Reliability considerations

- FDDI's reconfiguration capabilities

Theoretical Analysis – Publications

- Proof that Timing Requirements of the FDDI Token Ring Protocol are Satisfied

- Fairness of Channel Access for Non–Time–Critical Traffic Using the FDDI Token Ring Protocol

FDDI MAC protocol

- T__Opr — expected token rotation time

- TRT — token rotation timer

- TRT is reset when it expires and when the token arrives on time

- Synchronous transmission always allowed

- Asynchronous transmission only allowed to the extent that the token is ahead of schedule

Assumptions

- Each station uses full synchronous allocation

- S is total time for synchronous transmission during single cycle

- Infinite supply of asynchronous frames

- Asynchronous frame size is constant

- Stations abruptly cease transmission when timer expires

- No overhead

Extended cycle

1
2
•
•
m−1
⎡ m
⎢ m+1
⎢ •
⎢ •
⎢ n
⎢ 1
⎢ 2
⎢ •
⎢ •
⎢ m−1
⎣ m
m+1
•
•
n
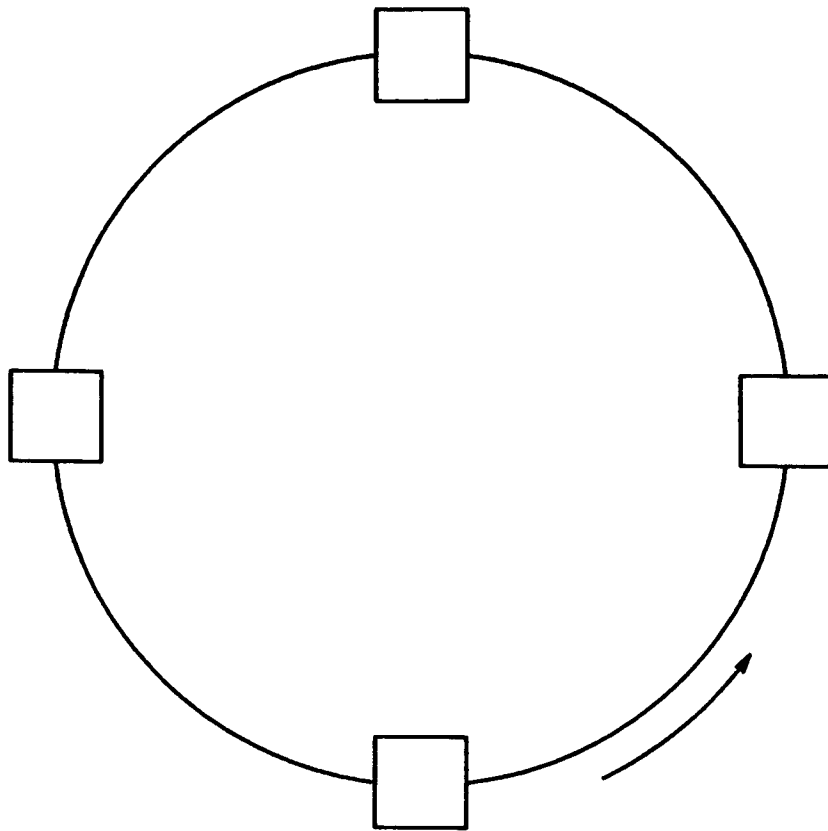
Consecutive extended cycles

$$
\left[
\begin{array}{c}
1 \\
2 \\
\bullet \\
\bullet \\
\left[
\begin{array}{c}
m-1 \\
m \\
m+1 \\
\bullet \\
\bullet \\
n \\
1 \\
2 \\
\bullet \\
\bullet \\
m-1
\end{array}
\right. \\
m \\
m+1 \\
\bullet \\
\bullet \\
n
\end{array}
\right.
$$

Asynchronous transmission pattern

- Asynchronous transmission time during extended cycle is exactly $T\_Opr - S$

- Asynchronous access time shifts cyclically around the ring

- Stations have equal access to transmit asynchronous frames

- Result is independent of relative sizes of individual stations' synchronous bandwidth allocations

Further results – taking asynchronous overrun into consideration

- If M > n, fairness of asynchronous access depends on asynchronous frame size

- If M < n, fairness cannot be guaranteed

M = maximum number of asynchronous frames during an extended cycle

n = number of stations

Maximum no. asynchronous frames during an extended cycle:

$$\lceil (T\_Opr - L - S - O)/A \rceil$$

L = lateness
S = synchronous transmission
O = overhead
A = asynchronous frame transmission time
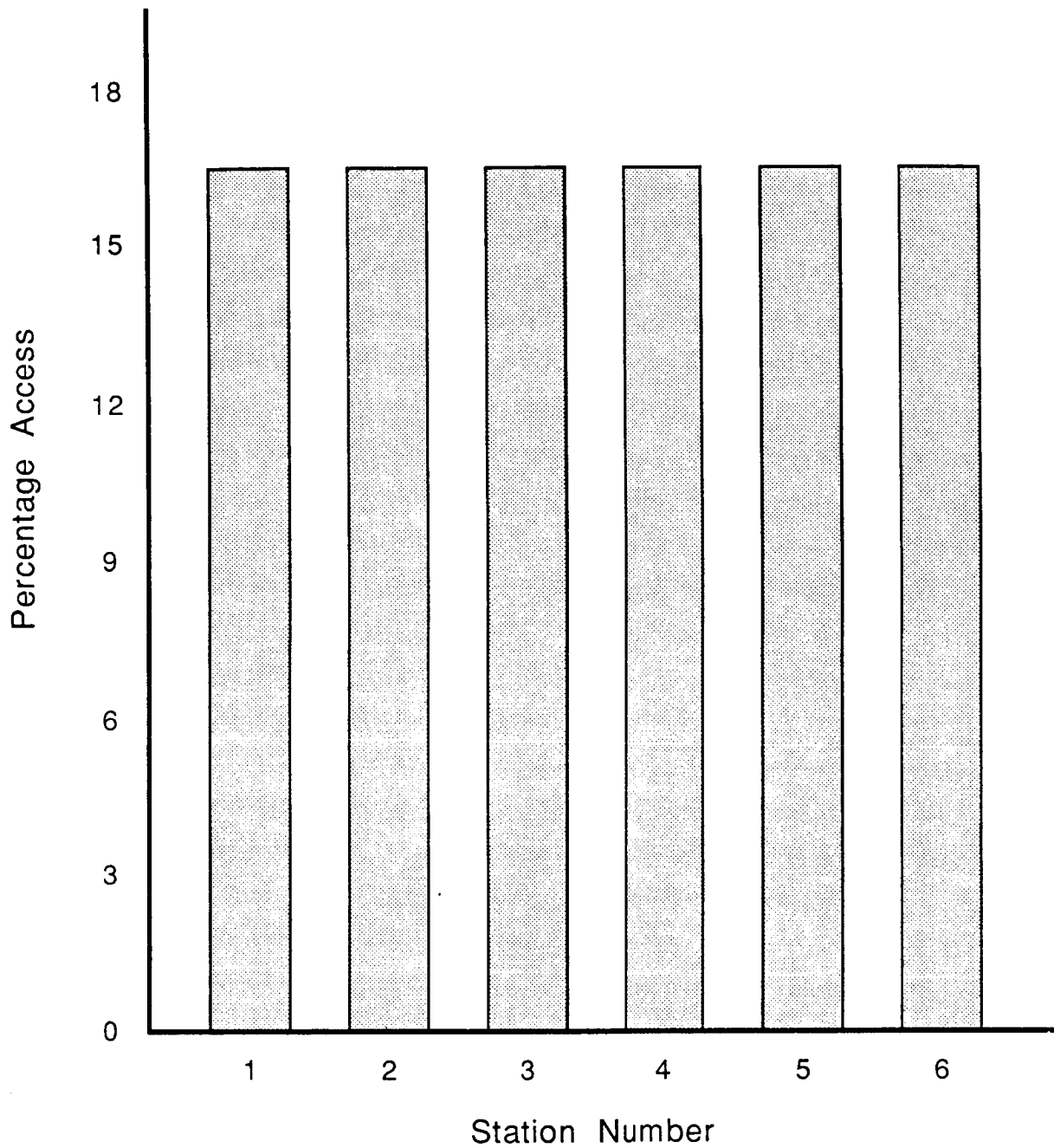
Channel Access for FDDI High
Bandwidth Token Ring
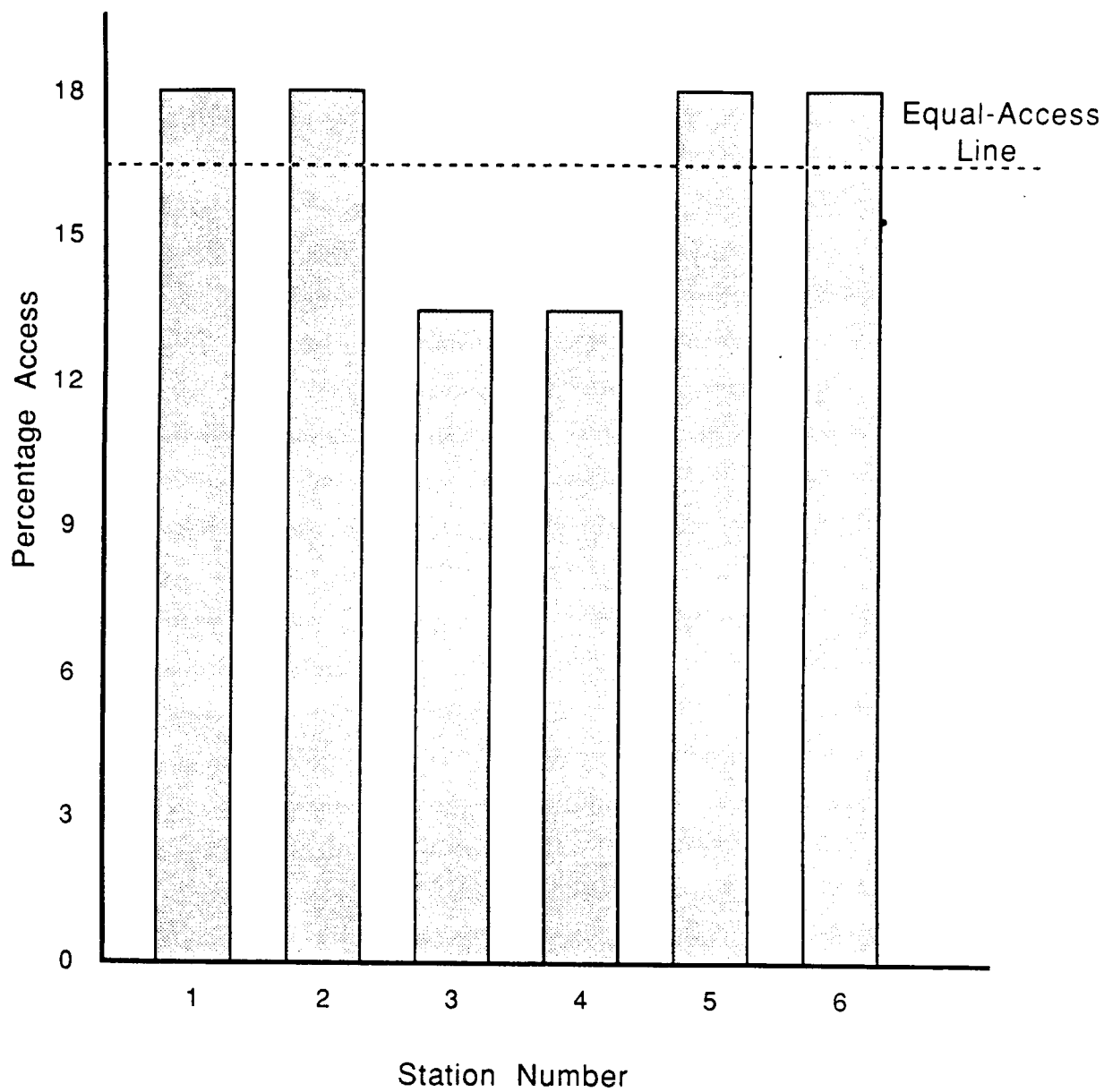
M > 6

Channel Access for FDDI High
Bandwidth Token Ring

M > 6
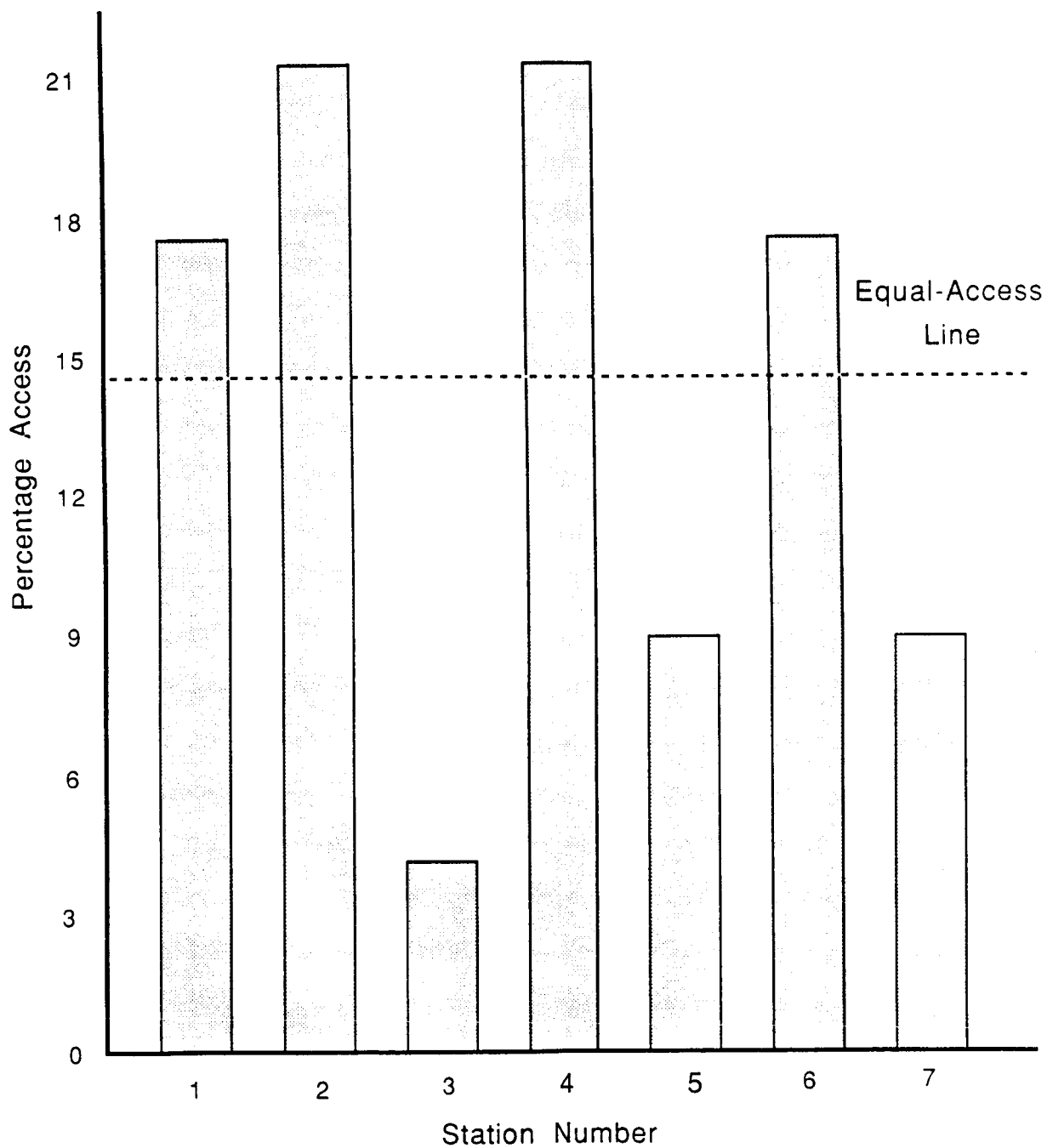
Channel Access for FDDI High Bandwidth
Token Ring

M < 7

Unfairness can be created by higher layer phenomena, such as buffer congestion

Access to Channel		
Station	Sync Transmission (%)	Async Transmission(%)
1	13	7.4
2	0	12.5
3	0	12.5
4	0	8.6
5	0	11.6
6	0	11.3

Application Study

- Problem

  Governmental agency application

- Desired results

  Determine response time

  Measure system degradation as increase workload

  Vary protocol parameters

- Method of study

  Used LANES
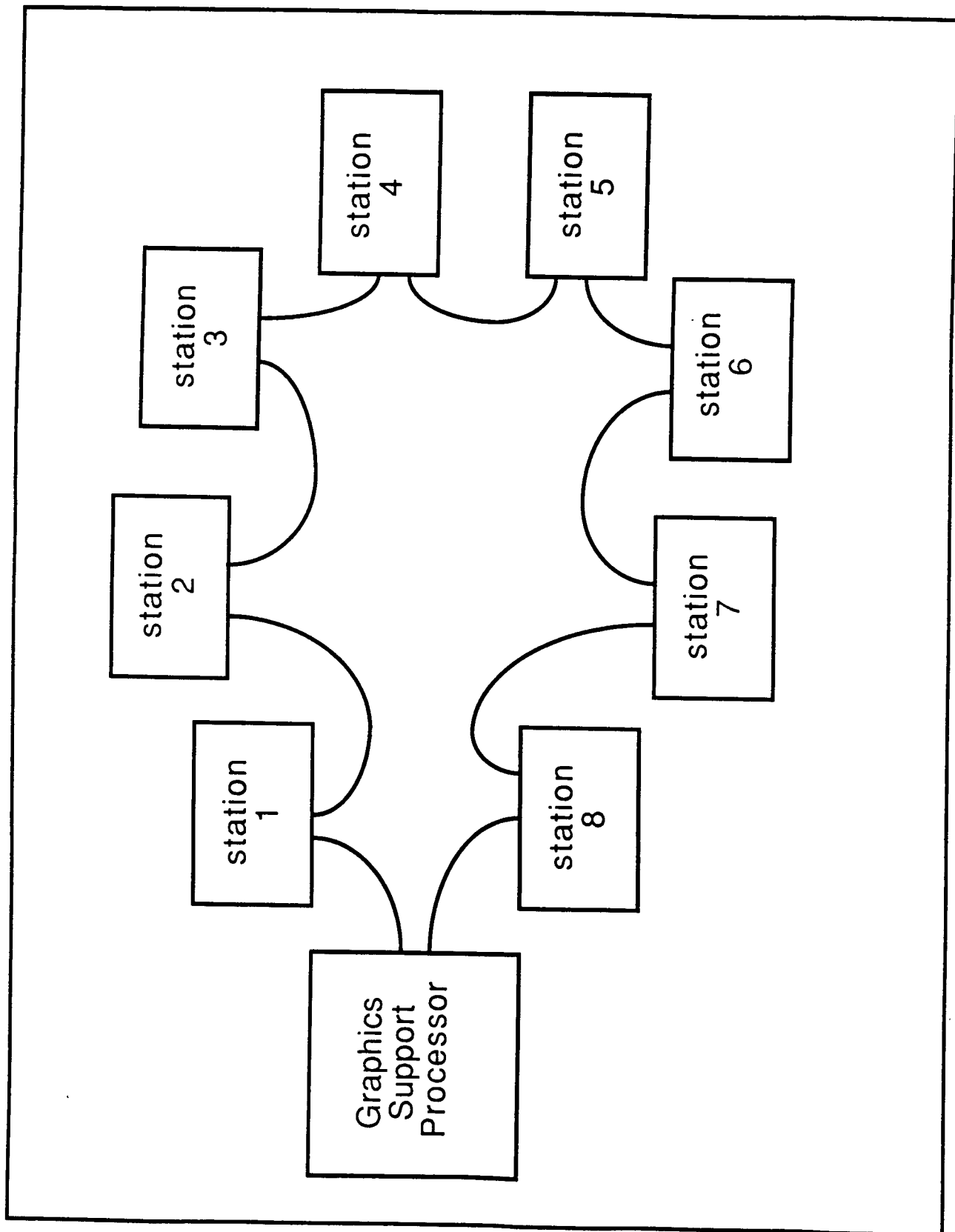
Future Studies

- Hold workshop to compare FDDI with SAE/AE—9B token ring protocol

- Determine how end application dictates communication requirements

- Study distributed system reconfiguration

STAR* BUS

J. Rende/GSFC

o   SYSTEM CHARACTERISTICS

o   ONGOING TASKS

o   SCHEDULE

o   SOME TEST RESULTS

STAR*BUS MAJOR CHARACTERISTICS

O LOCAL AREA NETWORK OF 32 REDUNDANT BUS INTERFACE UNITS (BIUs)

O SIMPLE, RELIABLE FIBER OPTIC TECHNOLOGY
  - LED EMITTER
  - PIN PHOTO DETECTOR
  - PASSIVE STAR COUPLER

O DISTRIBUTED BUS ACCESS PROTOCOL (CSMA/CD/TS)

O PACKETIZED DATA DISTRIBUTION

O LAYERED NETWORK MANAGEMENT

O BROADCAST BUS TOPOLOGY AT 100 MB/S

O BUS IMPACT IMMUNITY FROM USER TURN-ON, TURN-OFF, AND CHANGES

STAR*BUS TOPOLOGY
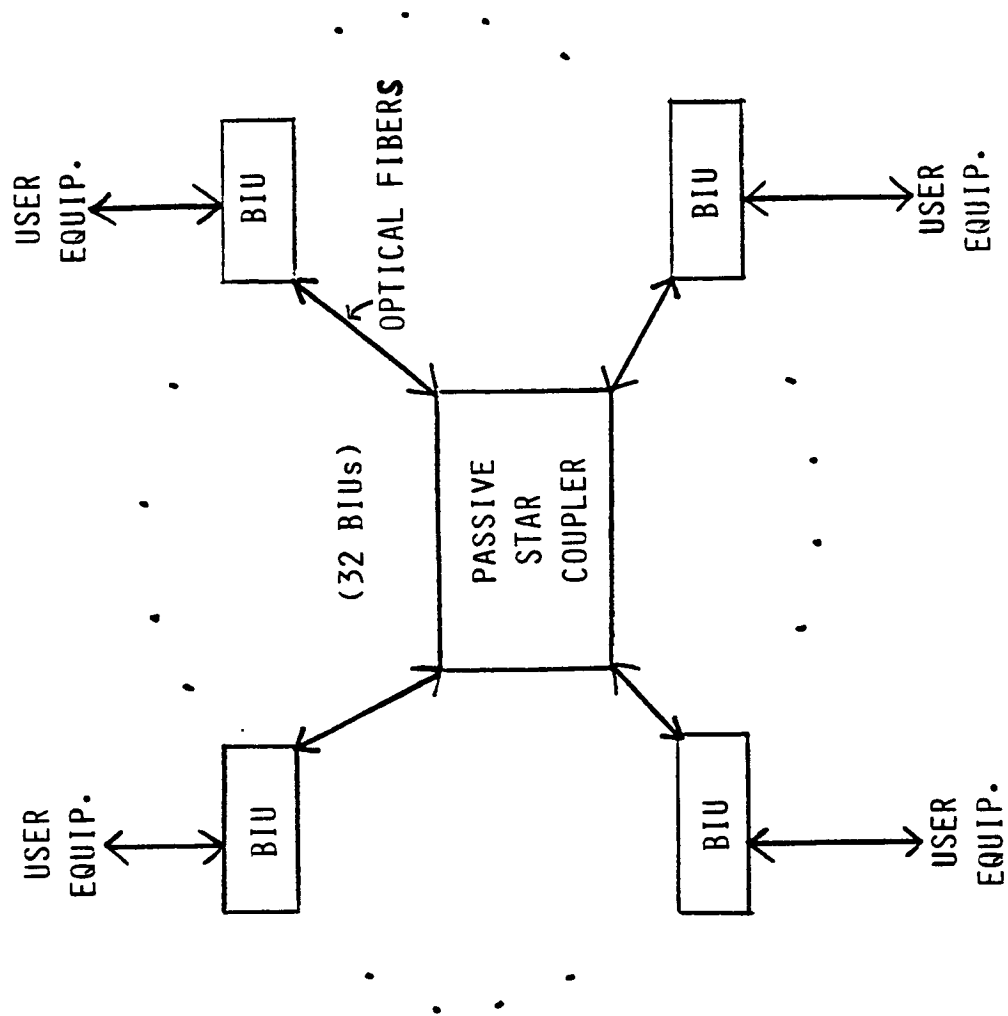
BIU ARCHITECTURE & DATA ROUTING
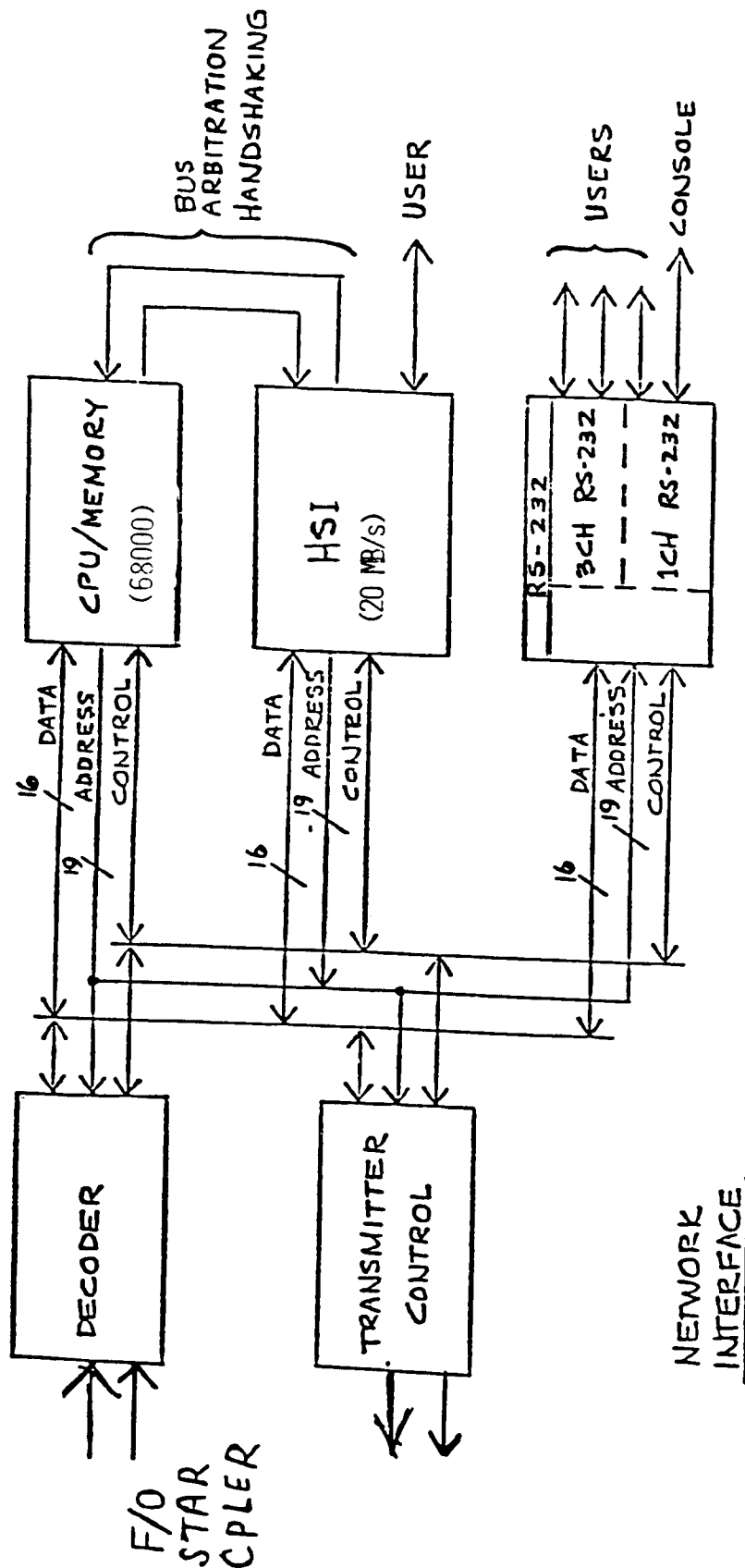
OPTICAL SIGNAL POWER BUDGET

LAUNCHED POWER	-3.0 DBM
TERMINATED CABLES	-2.0
32 X 32 WORST PATH	-18.0
COUPLER CONNECTORS	-1.5
DETECTOR COUPLING	-0.5
MIN SIGNAL LEVEL	-25.0
RCVR MIN DET SIGNAL	-27.0 @ BER < 10^{-8}
SYSTEM MARGIN	+2.0

2-89

OPTICAL BUS TRANSMITTER

o LIGHT SOURCE - AL GaAs LED MOTOROLA MFOE 1202

o LED CHARACTERISTICS

- PEAK EMISSION AT 815 NM

- OUTPUT SPOT DIAMETER IS 250 UM

- MINIMUM LAUNCHED POWER USING SCREENING IS 500 UW

o FOR I_F = 180 MA LED RISE TIME = 2 NS
  AFTER 50 METERS RISE TIME < 3.5 NS

OPTICAL RIIS RECEIVER

O .LIGHT DECTOR - PIN PHOTO DIOD RCA C30971E

O PIN CHARACTERISTICS

  - RESPONSITIVITY AT 815 UM IS .5 A/W

  - RISE, FALL TIMES = .5 NS

O RCVR SENSITIVITY = -27 DBM @ BER 10^{-8}

O DYNAMIC RANGE > 25 DB

PRESENT TASK: IMPLEMENT ISO LAYERS 3 AND 4

DESCRIPTION

0 INSTALL ISO STANDARDS TP4/IP

0 FILE TRANSFER, REMOTE LOGIN HOST APPLICATIONS

STATUS

0 BUI HARDWARE CHANGES TESTED

   INTERRUPT CONTROLLER

   EXPANDED MEMORY

0 SERIAL HIGH SPEED PORT ON HOST SUCCESSFULLY TESTED

   WITH TEST DATA

0 CODE BEING TESTED

PRESENT TASK: BUS INTERFACE UNITS - LSI INSERTION

<u>DESCRIPTION</u>

0   SUBSTITUTE GaAs GATE ARRAY FOR ECL FOR HIGH SPEED LOGIC
     FUNCTIONS IN DECODER

0   SUBSTITUTE CMOS GATE ARRAY FOR TTL LOGIC IN DECODER

FUNCTIONS IMPLEMENTED (GaAs)

     PACKET FLAG STRIPPING

     16 BIT SERIAL TO PARALLEL CONVERSION

     16 BIT POLYNOMIAL (CRC) DIVISION REGISTER

     16 BIT DATA LATCH

70 % DECREASED POWER CONSUMPTION PREDICTED

     LISTED FUNCTIONS PRESENTLY = 5 WATTS

     LISTED FUNCTIONS WITH GaAs SUBSTITUTION = 1.4 WATTS

<u>STATUS</u>

0   TEST VECTORS FOR GaAs GENERATED

0   CIRCUIT SIMULATION FOR GaAs SUCCESSFULLY TESTED UP
     450 MB/S

0   INITIAL STAGES OF GaAs CHIP FABRICATION UNDERWAY
     (SPERRY-TRIQUINT)

0   CMOS GATE ARRAY CKT SIMULATION UNDERWAY

C-2

DECODER A FUNCTIONS
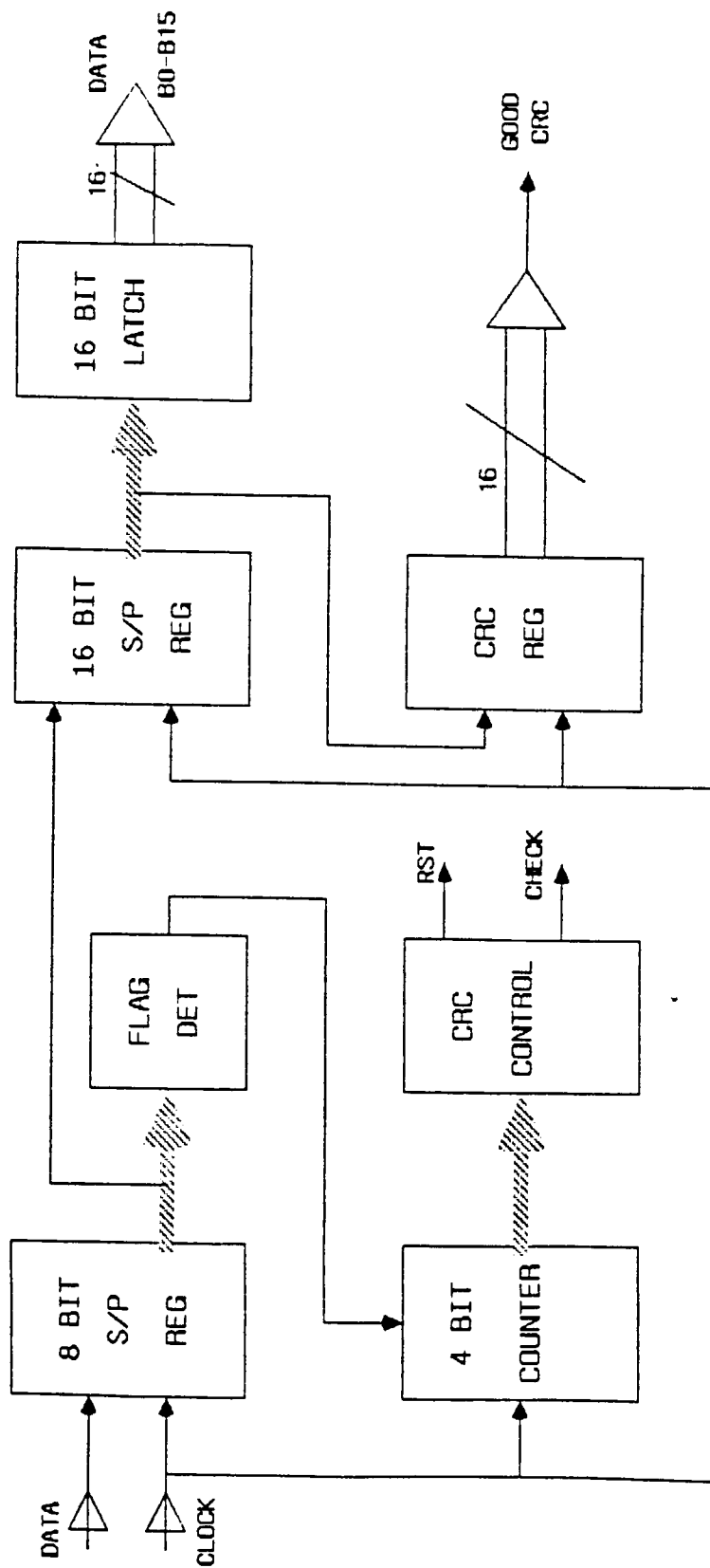
PRESENT TASK: NETWORK GATEWAY

TASK DESCRIPTION

- o INTERCONNECTS FDDI RING TO STAR*BUS

- o USES STAR*BUS BIU LAYERS 1 - 3

- o USES FDDI NIU LAYERS 1 - 3

- o ELECTRICAL INTERFACES TO SERIAL HIGH SPEED I/O

- o PROTOCOL INTERFACE AT LAYER 3

- o FRAGMENTATION

- o NODE ADDRESS MAPPING

- o COLLECT STATISTICS

TASK STATUS

- o CDR TO BE HELD IN NOVEMBER 1986

LAN CONNECTION

STAR * BUS

F/O

BIU HSI

ELECTR

GW

ELECTR

HSI NIU

F/O

FDDI RING
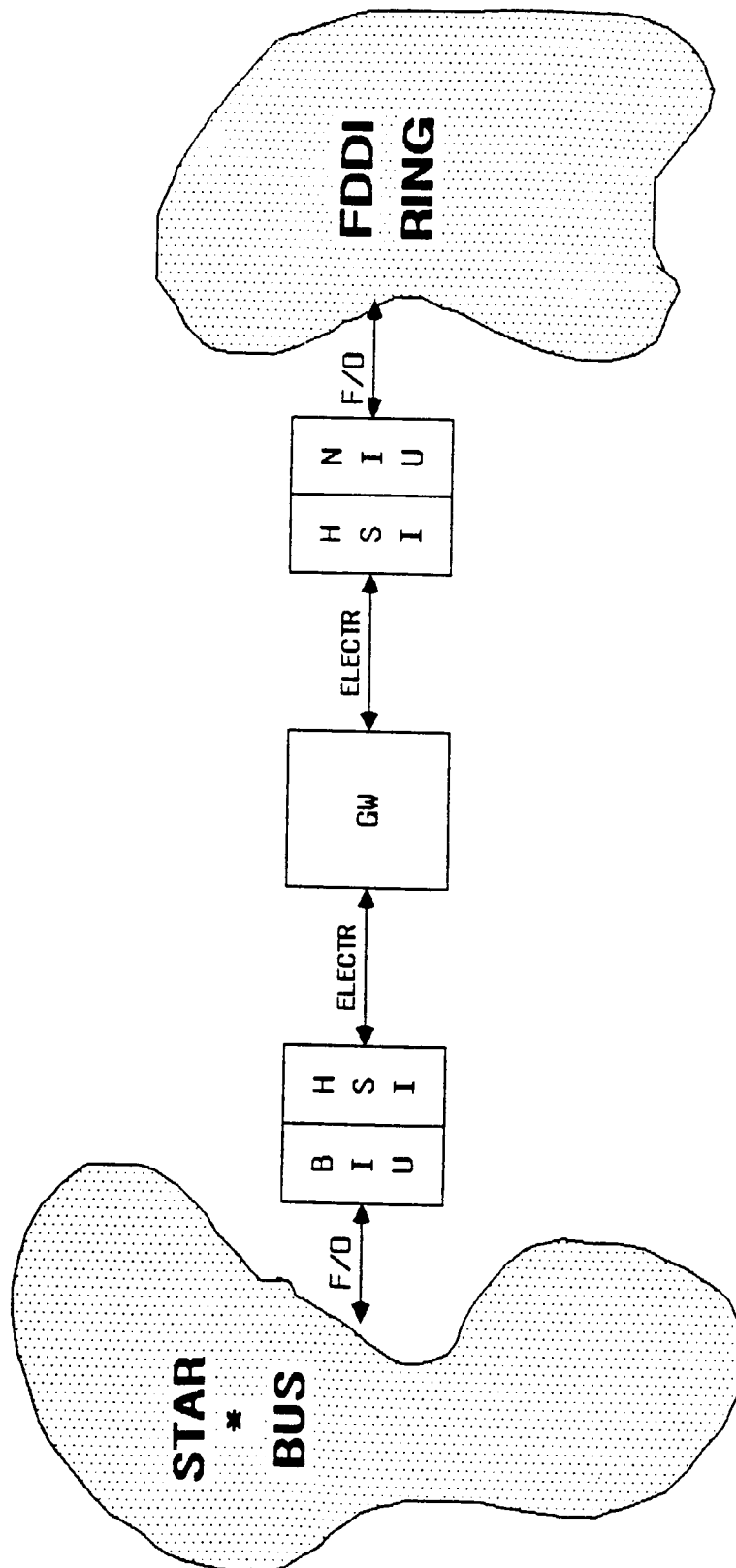
PRESENT TASK: CUSTOMER INTERFACE ADAPTER

DESCRIPTION

o   INTEGRATE A VARIETY OF MODULAR, POPULAR HARDWARE INTERFACES
     INTO A UNIT THAT FUNCTIONS WITH THE STAR*BUS BIU

o   THE UNIT WILL HAVE HIGH THROUGHPUT CHARACTERISTICS AND WILL
     FEATURE AN ADAPTABLE ARCHITECURE FOR INCORPORATING DATA
     MANAGEMENT LAYERS ONE AND TWO IN FUTURE DESIGNS

STATUS

o   CONTRACT WITH FAIRCHILD SPACE COMPANY

o   PHASE ONE IS GATHERING INPUTS FORM POTENTIAL USERS AND DMS
     INTERESTED PARTIES

o   PHASE TWO IS DESIGN, FABRICATION AND TESTING

CIA BLOCK DIAGRAM

TO BIU

SHSI

TX DUAL PORT MEM

RX DUAL PORT MEM

CPU

V M E   B U S

I/O MODULE

USER 1

I/O MODULE

USER N
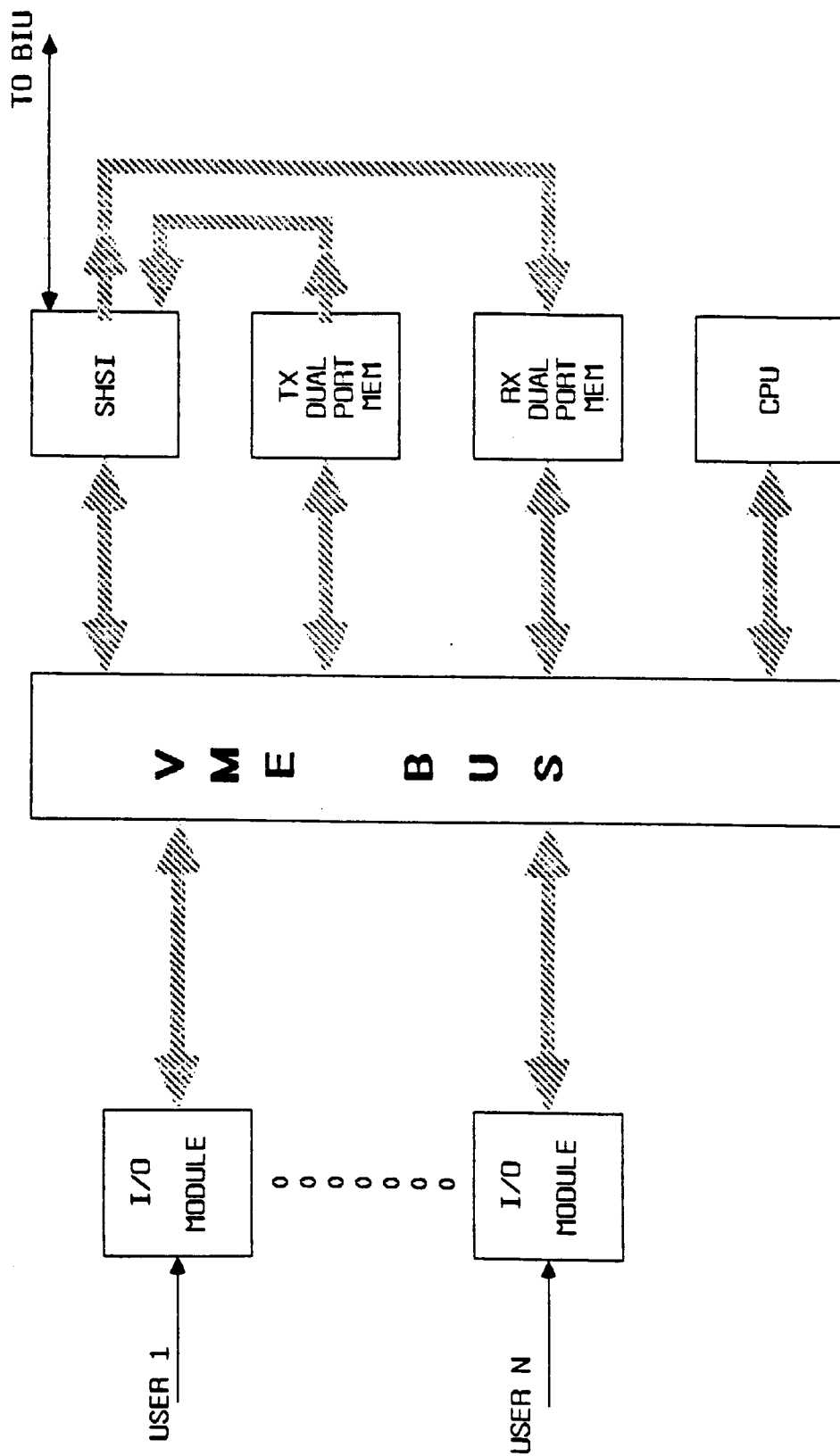
ITERIM BIU-USER STRUCTURE

RS232, RS422/449
2MB/S (DMA)
HOSTS, WORKSTATIONS

2 MB/S (DMA)
VIDEO (SLOW FRAME)

INSTRUMENTS

IEEE 488 (PARALLEL)
RS-232 (SERIAL)

BIU

N	F	H
I	E	S
U	P	I

H	C
S	I
I	A

32 MB/s
BURSTS

F/O
NETWORK
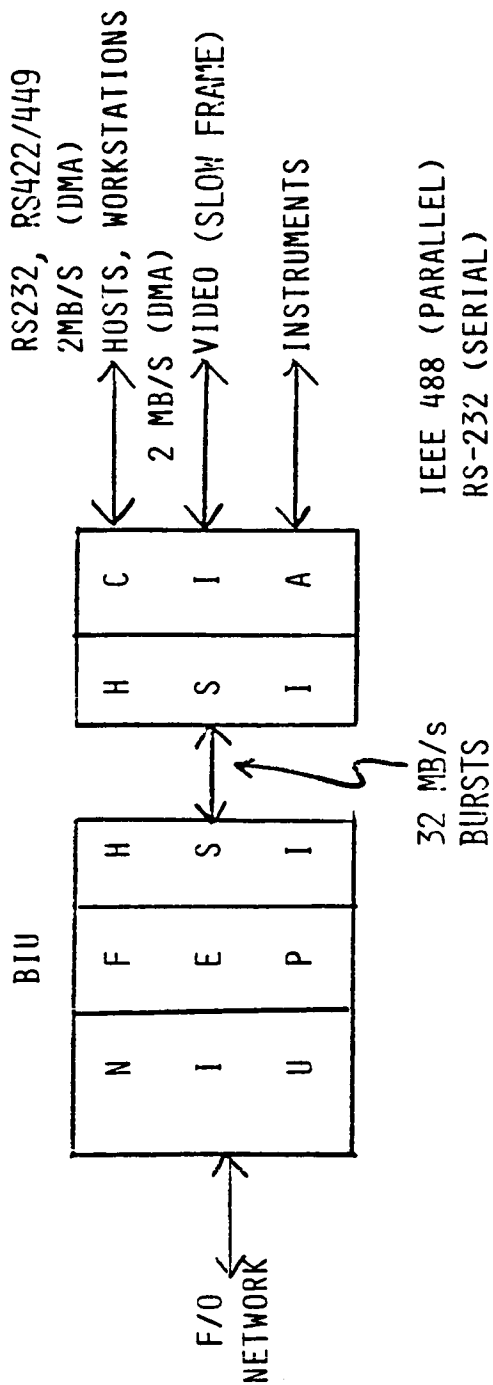
STAR * BUS IN JSC
DMS TEST BED

PERIPHERALS

HOST COMPUTER
- UNIX OS
- NSTL P/L SIM
- APPL PROC'S

SHSI

BIU 2.
- GAAS VLSI
- TRANSPORT PROTOCOL

TERM

BIU 3.

SHSI

NETWORK GATEWAY

TERM

FDDI CORE 'RING'

fiber

(20 mb/s)
EXER DATA

SHSI

BIU 1.

TERM

20X20 COUPLER

NETWORK MONITOR-EXER 6.

GRAPHICS DISPLAY

TERM

EXER DATA
(20 mb/s)

RS170 RS170
TV MON VCR

CUSTOMER INTERFACE ADAPTER

IEEE/488
INSTRUMENTS

SHSI

BIU 5.

COMMAND GENERATOR

RS-422/449
CCSDS
SOURCE
PAC

H/W P/L SIM

TERM

BIU 4.

SHSI

EXER DATA
(20 mb/s)

RS 232

HOST COMPUTER

PERIPHERALS

TERM

MILESTONES

1988
JAN

OCT

JUL

APR

1987
JAN

GAAs INSERT, TEST

NET COMM PROT
INSTALL, TEST

NETWORK GATEWAY
INTEGRATE, TEST

NSTL P/L SIM
INSTALL, TEST

CUSTOMER INTERFACE
ADAPTER INTEGRATE,
TEST

STAR*BUS INSTALL
JSC

PERFORMANCE EVALUATION

TEST SET-UP

STATISTICS

BIU
1

BIU
2

BIU
3

STAR
COUPLER

APD
DET

DATA
GENERATOR

BIU
4

STATISTICS

STATISTICS

STATISTICS

STATISTICS

32 MB/s
SERIAL BURSTS

o VARYING PACKET SIZES
o END-TO-END ERROR CHECK

2-103
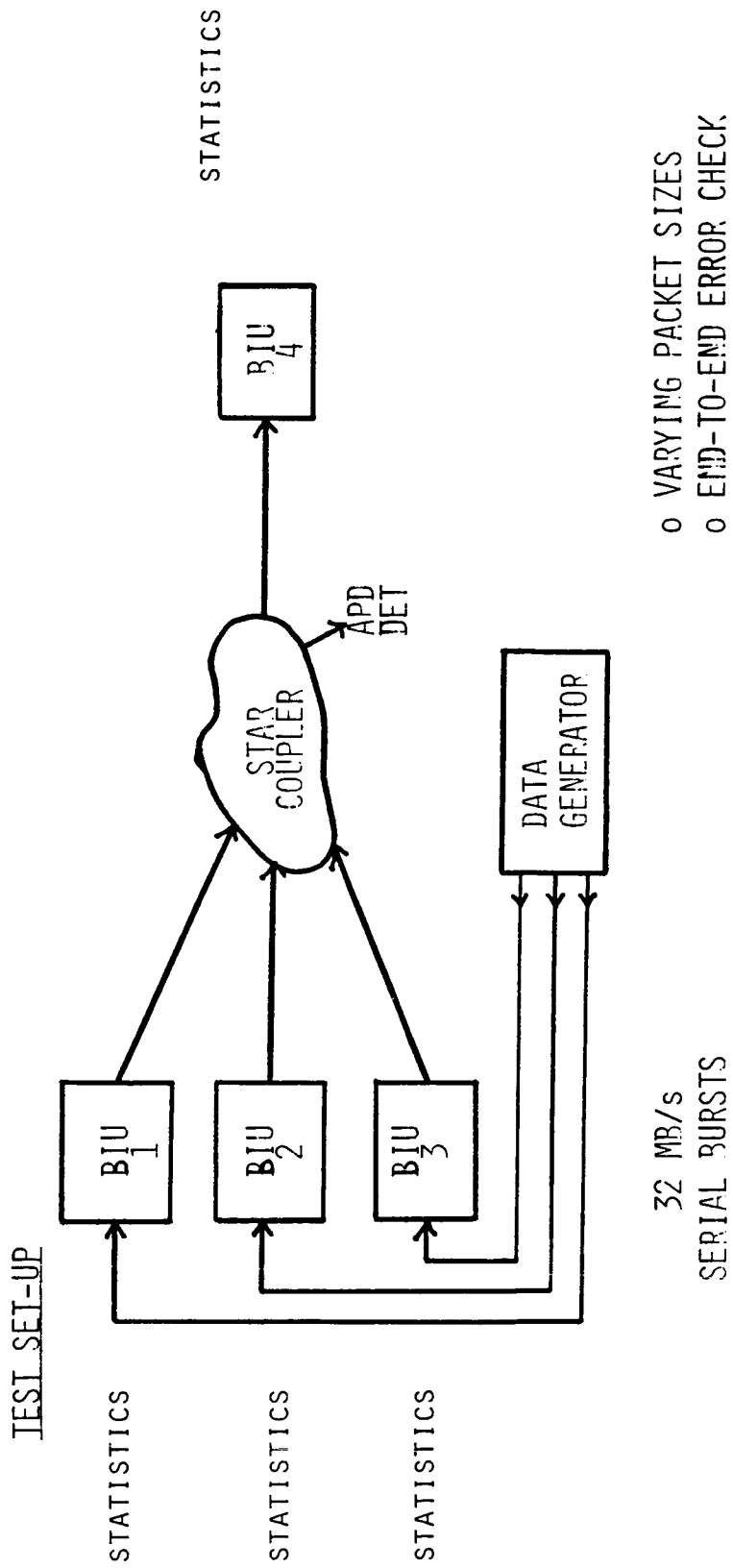
A. DATA GATHERED

    O BUFFER-FULL STATISTICS ON RECEIVING BIU

    (QUEUE SIZE = 1) VERSUS OFFERED TRAFFIC

    O COLLISION RATE ON FIBER OPTIC BUS VERSUS

    OFFERED TRAFFIC

B. RESULTS COMPARED TO POISSON DISTRIBUTION MODEL

$$P(BF) = \frac{\rho}{1+\rho}$$

PERCENT

PACKETS
REJECTED
DUE TO
QUEUE
FULL

OFFERED TRAFFIC
MB/S

PERCENT

COLLI-
SIONS

OFFERED TRAFFIC
MB/S

2-106
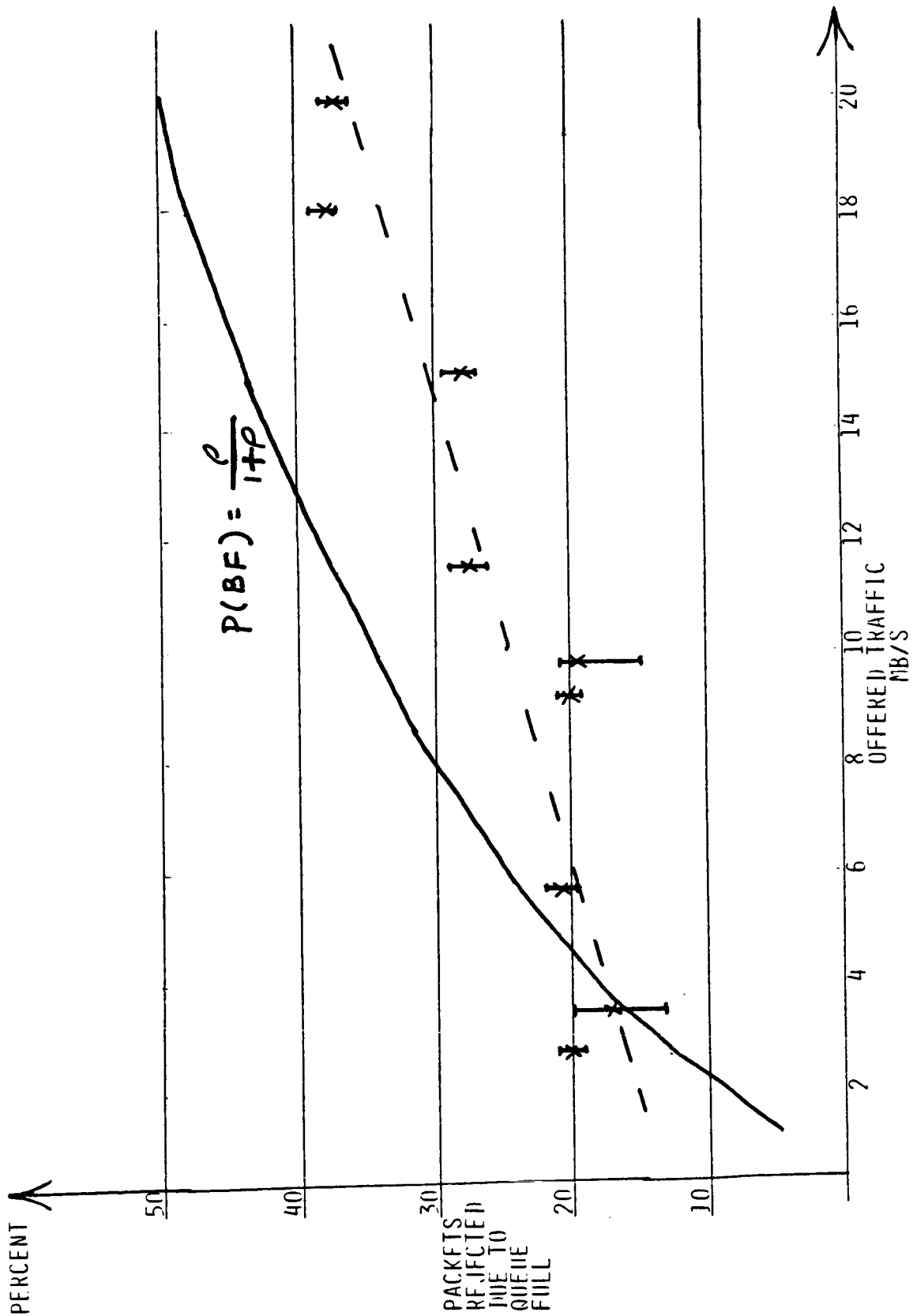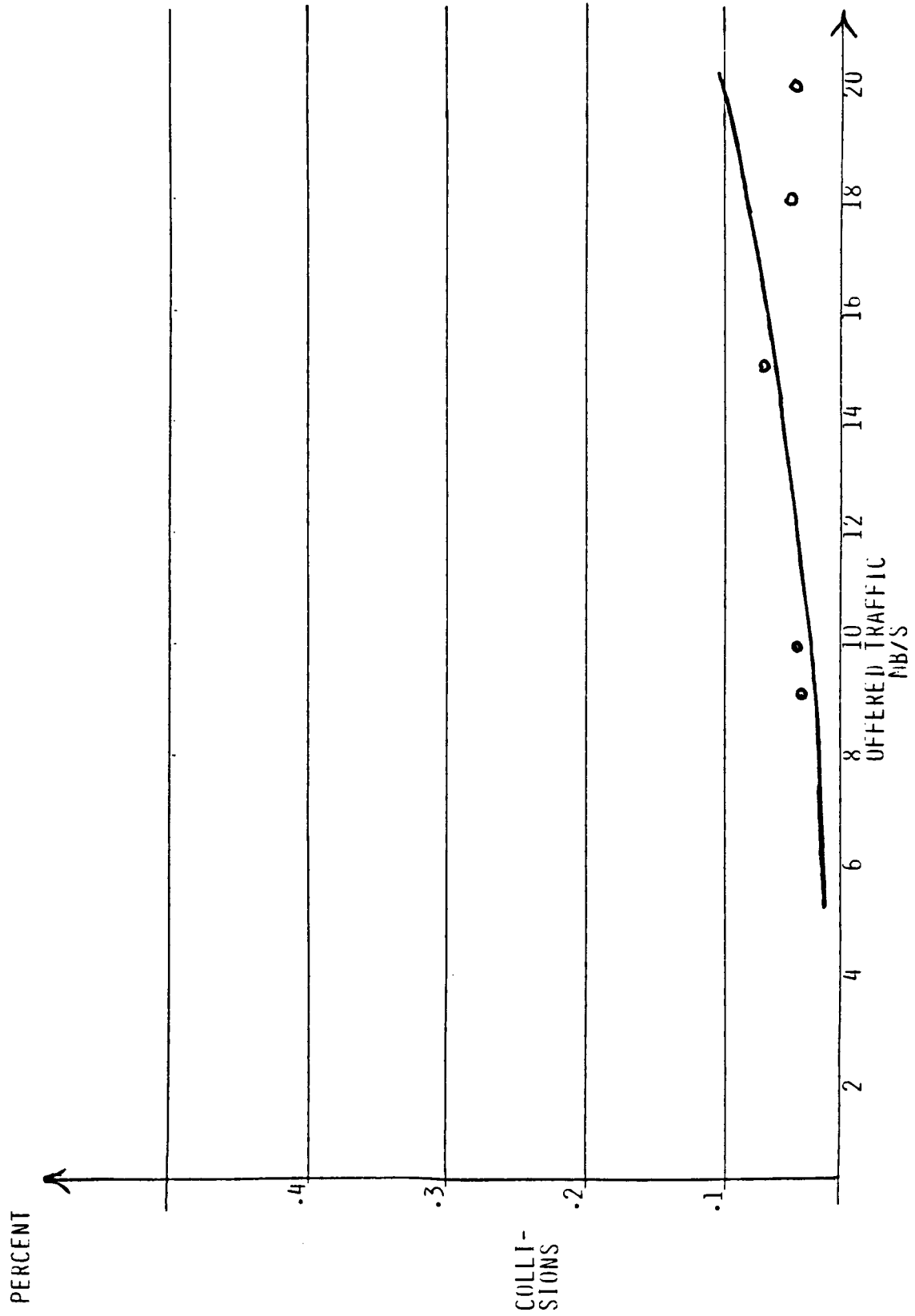
A Distributed Processing Network Simulator (DPNS)

Silvano Colombano (project leader)
Karyn Weinstein   (programmer)
Sharon Doubek   (user interface)
Donald Dubois   (ECSS consultant)

Terry Grant   (project monitor)

OUTLINE

- Purpose of project

- System description

- Output reports

- Applications

- Sample scenarios

- User interface

- Future development

Purpose of the Project:
SIMULATION OF THE SSIS
UNDER REALISTIC WORKLOAD
CONDITIONS

SSIS USER: establish whether the SSIS environment meets user requirements

- system availability

- running times

SSIS DESIGNER: find potential bottlenecks

- effects of different hardware configurations

- effects of different ISO/OSI protocols

SIMULATION RESEARCH: increase the usefulness of simulation tools

- user interfaces

- model based expert systems

- automatic workload management

System Description

Language: ECSS (Simscript)

Defined at run-time

- Network architecture

- Workload characteristics

Compiled

- Foreground job structure

- Background job structure

Network Architecture

Network topology

- Nr. of LANs

- Connectivity

- Bridges and gateways

For each LAN

- Nr. of nodes

- ISO/OSI protocols

For each node

- Devices (type and quantity)

For each device

- Characteristics (ex. execution rates, transmission rates, latency, etc.)

System definition: Nodal Physical Device Configuration

— NODAL PHYSICAL DEVICE CONFIGURATIONS —

PHYSICAL DEVICE NAME	NO. OF DEVICES	EXECUTION/TRANSMISSION RATE DEFAULT	USER SPECIFIED	DATA UNIT	ACCESS LATENCY (SECS)
LAN # 1					
NODE # 1					
TAPE.DRIVE	2	+2.00E+06	+2.00E+06	BYTES/SEC	3.000
DISK.DRIVE	3	+4.00E+06	+4.00E+06	BYTES/SEC	0.500
PROCESSOR	1	+2.00E+06	+2.00E+06	INSTRUCTIONS/SEC	0.
DISPLAY	2	19000.000	19000.000	BITS/SEC	1.000
INSTRUMENT	1	+2.00E+06	+2.00E+06	BITS/SEC	0.
CLOCK	1	100.000	100.000	BITS/SEC	0.
SENSOR	3	5000.000	5000.000	BITS/SEC	0.
VOICE	1	16000.000	16000.000	BITS/SEC	3.000
VIDEO	1	+2.20E+07	+2.20E+07	BITS/SEC	0.
PRINTER	1	100.000	100.000	BYTES/SEC	3.000
NODE # 3					
TAPE.DRIVE	4	+2.00E+06	+2.00E+06	BYTES/SEC	3.000
DISK.DRIVE	5	+4.00E+06	+4.00E+06	BYTES/SEC	0.500
PROCESSOR	1	+2.00E+06	+2.00E+06	INSTRUCTIONS/SEC	0.
DISPLAY	2	19000.000	19000.000	BITS/SEC	1.000
INSTRUMENT	6	+2.00E+06	+2.00E+06	BITS/SEC	0.
CLOCK	1	100.000	100.000	BITS/SEC	0.
SENSOR	3	5000.000	5000.000	BITS/SEC	0.
VOICE	1	16000.000	16000.000	BITS/SEC	3.000
VIDEO	1	+2.20E+07	+2.20E+07	BITS/SEC	0.
PRINTER	1	100.000	100.000	BYTES/SEC	3.000
LAN # 2					
NODE # 1					
TAPE.DRIVE	1	+2.00E+06	+2.00E+06	BYTES/SEC	3.000
DISK.DRIVE	1	+4.00E+06	+4.00E+06	BYTES/SEC	0.500
PROCESSOR	1	+2.00E+06	+2.00E+06	INSTRUCTIONS/SEC	0.
DISPLAY	1	19000.000	19000.000	BITS/SEC	1.000
INSTRUMENT	1	+2.00E+06	+2.00E+06	BITS/SEC	0.
CLOCK		100.000	100.000	BITS/SEC	0.

System definition: Nodal Logical Device Configuration

— NODAL LOGICAL DEVICE CONFIGURATIONS —

LOGICAL DEVICE NAME   PHYSICAL DEVICE TYPE

LAN # 1

NODE # 1

Logical Device Name	Physical Device Type
SS.PAYLOAD.UTILITIES.SENSORS	SENSOR
REAL.TIME.CLOCK	CLOCK
SSDS	INSTRUMENT
TAPE.DRIVE1	TAPE.DRIVE
DISK.DRIVE1	DISK.DRIVE

NODE # 3

Logical Device Name	Physical Device Type
DISPLAY	DISPLAY
RECORDER	VOICE
CUSTOMER.TAPE	TAPE.DRIVE
SS.PAYLOAD	INSTRUMENT
TAPE.DRIVE2	TAPE.DRIVE
DISK.DRIVE2	DISK.DRIVE

LAN # 2

NODE # 1

Logical Device Name	Physical Device Type
PAYLOAD.TEST.UNIT	INSTRUMENT
SS.PAYLOAD.PLATFORM	INSTRUMENT
PAYLOAD.MONITORING.SENSORS	SENSOR
PAYLOAD.CHECK.UNIT	INSTRUMENT
TAPE.DRIVE3	TAPE.DRIVE
DISK.DRIVE3	DISK.DRIVE

NODE # 2

Logical Device Name	Physical Device Type
CUSTOMER.MMI	DISPLAY
SENSORS	SENSOR
SS.PORT.ROT.UNIT	INSTRUMENT
TAPE.DRIVE4	TAPE.DRIVE
DISK.DRIVE4	DISK.DRIVE

2-113

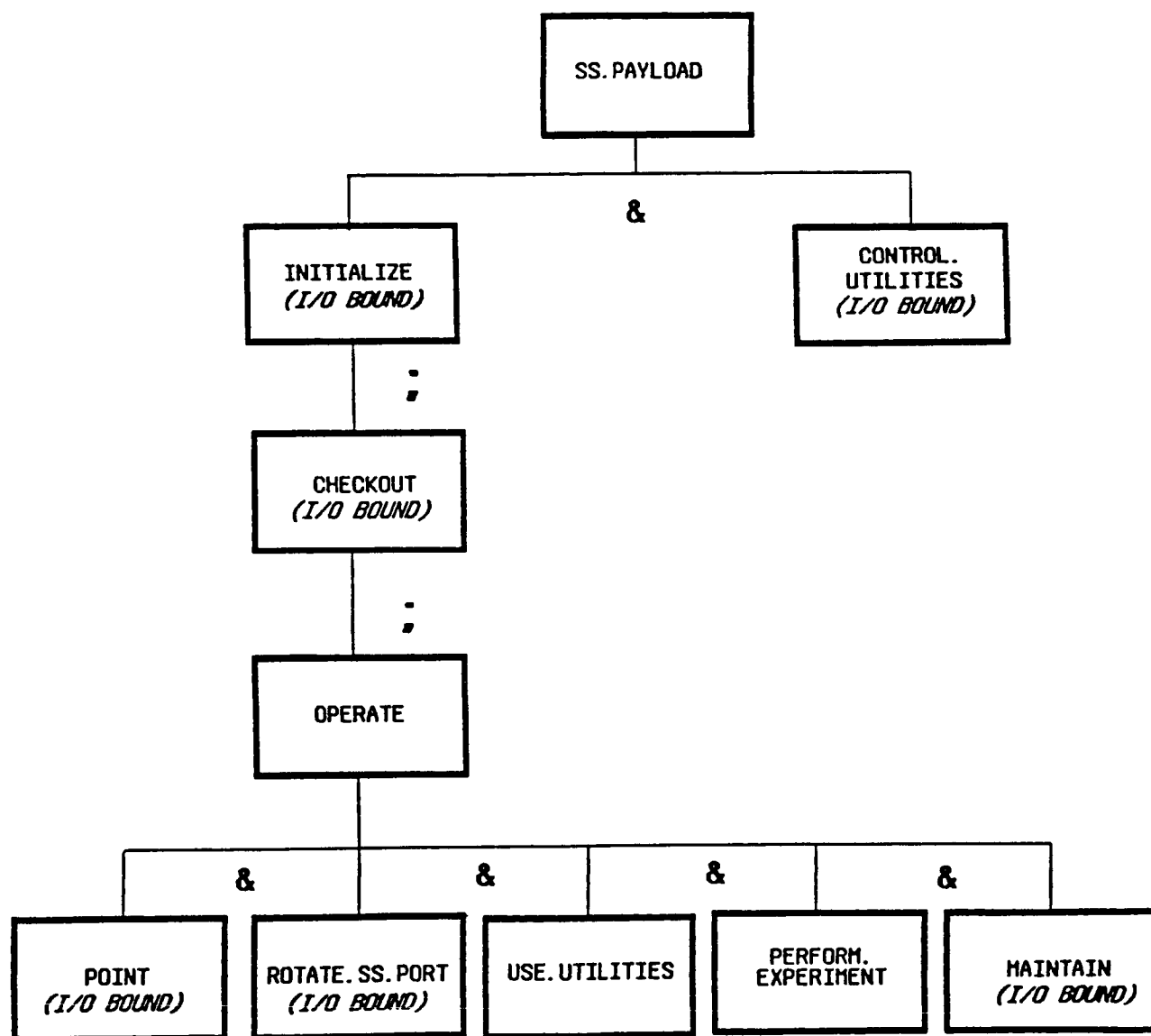# User Defined Workload Characteristics

Foreground job

- Location of job and subjobs

- Logical devices used

- Nr. of instructions for each subjob

- Assignment of logical devices to physical devices

- Amount of I/O to/from I/O bound subjobs

Background jobs

- Frequency of job initiation (uniform random distribution throughout the network)

System definition: Foreground Job Structure

```
                          ┌─────────────────┐
                          │   SS.PAYLOAD    │
                          └─────────────────┘
                    ┌──────────────&──────────────┐
          ┌─────────────────┐              ┌─────────────────┐
          │    INITIALIZE   │              │    CONTROL.     │
          │    (I/O BOUND)  │              │    UTILITIES    │
          └─────────────────┘              │    (I/O BOUND)  │
                   ;                        └─────────────────┘
          ┌─────────────────┐
          │    CHECKOUT     │
          │   (I/O BOUND)   │
          └─────────────────┘
                   ;
          ┌─────────────────┐
          │     OPERATE     │
          └─────────────────┘
```

```
      &            &            &            &
┌──────────┐ ┌──────────────┐ ┌────────────┐ ┌────────────┐ ┌────────────┐
│  POINT   │ │ROTATE.SS.PORT│ │USE.UTILITIES│ │  PERFORM.  │ │  MAINTAIN  │
│(I/O BOUND)│ │ (I/O BOUND) │ │            │ │ EXPERIMENT │ │ (I/O BOUND)│
└──────────┘ └──────────────┘ └────────────┘ └────────────┘ └────────────┘
```

```
┌─────────────────────────────────────┐
│        JOB  HIERARCHY LEGEND         │
├─────────────────────────────────────┤
│    ;     SEQUENTIAL EXECUTION        │
│                                      │
│    &     PARALLEL EXECUTION          │
└─────────────────────────────────────┘
```

System definition: Workload Job Mappings

SYSTEM DEFINITION

— WORKLOAD JOB MAPPINGS —

MAPPED JOB/SUBJOB NAME	MAIN JOB
LAN # 1	
NODE # 1	
SS.PAYLOAD	SS.PAYLOAD
CONTROL.UTILITIES	SS.PAYLOAD
NODE # 3	
INITIALIZE	SS.PAYLOAD
CHECKOUT	SS.PAYLOAD
LAN # 2	
NODE # 1	
OPERATE	SS.PAYLOAD
POINT	SS.PAYLOAD
MAINTAIN	SS.PAYLOAD
NODE # 2	
ROTATE.SS.PORT	SS.PAYLOAD
USE.UTILITIES	SS.PAYLOAD
PERFORM.EXPERIMENT	SS.PAYLOAD

System definition: Job description

S Y S T E M   D E F I N I T I O N

JOB DESCRIPTION FOR CONTROL.UTILITIES

CPU INSTRUCTIONS EXECUTED: +8.00E+06

————— JOB INPUTS —————

ID	SOURCE	SIZE (BYTES)
SS.PAYLOAD.UTILITIES.STATUS	SS.PAYLOAD.UTILITIES.SENSORS	1700.000
TIME	REAL.TIME.CLOCK	4.000
SS.PAYLOAD.UTIL.DIRECTIVES	SSDS	1700.000
SS.PAYLOAD.UTIL.DIRECTIVES	CUSTOMER.MMI	1700.000

————— JOB OUTPUTS —————

ID	DESTINATION	SIZE (BYTES)
SS.PAYLOAD.UTILS.CMDS	DISPLAY	1700.000
SS.PAYLOAD.UTILS.CMDS	RECORDER	1700.000
SS.PAYLOAD.UTILS.CMDS	SSDS.DB1	1700.000

Output Reports

System definition (input)

System reports (avrg., max. and s.d. of all relevant values)

- Execution

- Processor utilization

- Queues

- Transmission

Job reports (avrg., max. and s.d. of all relevant values)

- Nr. of instances and completed instances

- Instance length

- Time executing, transmitting and blocked

Output report: Processor Execution

— EXECUTION REPORT —

DEVICE NAME	TOTAL EXECUTION TIME	JOB NAME	JOB EXECUTION TIME	% OF DEVICE EXECUTION
LAN # 2				
NODE # 1				
PROCESSOR # 1	190.000000	OPERATE	5.000000	2.632
		POINT	20.000000	10.526
		MAINTAIN	30.000000	15.789
		BG.PAYLOAD	5.000000	2.632
		BGINITIALIZE	10.000000	5.263
		BGCHECKOUT	20.000000	10.526
		BGPOINT	20.000000	10.526
		BGMAINTAIN	30.000000	15.789
		BGROTATE.SS.	45.000000	23.684
		BGPERFORM.EX	5.000000	2.632
NODE # 2				
PROCESSOR # 1	114.900000	ROTATE.SS.PO	45.000000	39.164
		PERFORM.EXPE	5.000000	4.352
		READ.DB	0.800000	0.696
		WRITE.DB	1.100000	0.957
		BGINITIALIZE	10.000000	8.703
		BGCHECKOUT	10.000000	8.703
		BGOPERATE	5.000000	4.352
		BGMAINTAIN	30.000000	26.110
		BGCONTROL.UT	8.000000	6.963
PROCESSOR # 2	86.400000	USE.UTILITIE	5.000000	5.787
		READ.DB	0.700000	0.810
		WRITE.DB	0.700000	0.810
		BG.PAYLOAD	5.000000	5.787
		BGINITIALIZE	10.000000	11.574
		BGCHECKOUT	20.000000	23.148
		BGPOINT	40.000000	46.296
		BGUSE.UTILIT	5.000000	5.787

Output report: Processor Utilization

S I M U L A T I O N   S T A T I S T I C S

FROM   0.   TO   +1.0E+03

—— PROCESSOR UTILIZATION REPORT ——

DEVICE NAME	NUMBER OF ACTIVATIONS	UTILIZATION TIME AVERAGE	UTILIZATION TIME MAXIMUM	% TIME UTILIZED
LAN # 1				
NODE # 1				
PROCESSOR # 1	51	3.078431	45.000000	15.700
NODE # 3				
PROCESSOR # 1	76	2.778947	45.000000	21.120
LAN # 2				
NODE # 1				
PROCESSOR # 1	24	7.916667	45.000000	19.000
NODE # 2				
PROCESSOR # 1	56	2.051786	45.000000	11.490
PROCESSOR # 2	44	1.963636	20.000000	8.640

Output report: Job SS.PAYLOAD

S I M U L A T I O N   S T A T I S T I C S

FROM   0.   TO   +1.0E+03

JOB REPORT FOR SS.PAYLOAD
LAN # 1   NODE # 1
FROM   0.   TO 1000.00

TOTAL NUMBER OF INSTANCES	1
NUMBER OF COMPLETED INSTANCES	1
AVERAGE INSTANCE LENGTH	896.151726
STANDARD DEVIATION INSTANCE LENGTH	0.
MAXIMUM INSTANCE LENGTH	896.151726
TOTAL LENGTH OF INSTANCES	896.151726

	TIME PER INSTANCE				% TOTAL
	AVERAGE	STD DEV	MAXIMUM	TOTAL	INSTANCE LENGTH
EXECUTION	5.000000	0.	5.000000	5.000000	0.558
TRANSMISSION	0.	0.	0.	0.	0.
BLOCKED FOR LOADING	0.	0.	0.	0.	0.
BLOCKED FOR ACTIVATION	0.	0.	0.	0.	0.
BLOCKED FOR TRANSMISSION	0.	0.	0.	0.	0.
BLOCKED FOR ALLOCATION	0.	0.	0.	0.	
BLOCKED FOR STORAGE	0.	0.	0.	0.	

Output report: Job READ.DB

JOB REPORT FOR READ.DB
FROM   0.   TO 1000.00

TOTAL NUMBER OF INSTANCES	29
NUMBER OF COMPLETED INSTANCES	29
AVERAGE INSTANCE LENGTH	22.406864
STANDARD DEVIATION INSTANCE LENGTH	16.732319
MAXIMUM INSTANCE LENGTH	55.599895
TOTAL LENGTH OF INSTANCES	649.799042

| | TIME PER INSTANCE | | | | % TOTAL |
	AVERAGE	STD DEV	MAXIMUM	TOTAL	INSTANCE LENGTH
EXECUTION	0.100000	0.000000	0.100000	2.900000	0.446
TRANSMISSION	10.031642	0.052676	10.125000	290.917625	44.770
BLOCKED FOR LOADING	0.	0.	0.	0.	0.
BLOCKED FOR ACTIVATION	8.554998	15.381331	45.498645	248.094942	38.180
BLOCKED FOR TRANSMISSION	13.751866	9.311171	54.606586	398.804100	61.373
BLOCKED FOR ALLOCATION	0.	0.	0.	0.	0.
BLOCKED FOR STORAGE	0.	0.	0.	0.	0.

Applications Planned

Design evaluation aid

- DMS design from work package 2

- DMS test-bed design

- System autonomy studies at ARC

- Parallel processing concepts at ARC

Operations planning and evaluation

- Operational LANs at ARC

Example: three scenarios

SCENARIO 1	SCENARIO 2	SCENARIO 3
1 LAN Localized FG	1 LAN Distributed FG	2 LANs Distributed FG

DPNS VERSION 2.0
SCENARIO 1

NODE 1
FG JOBS
BG JOBS
DB
CPU

NODE 4
BG JOBS
DB
(2)CPU

NODE 2
FG JOBS
BG JOBS
DB
CPU

NODE 3
BG JOBS
DB
CPU

NIU — LAN 1 — NIU

SYSTEM DATA PROCESSING DEVICE LEGEND

| MASS STORAGE | | INSTRUMENT | |
| DISPLAY | | PROCESSOR | CPU |

DPNS VERSION 2.0
SCENARIO 2

NODE 1

FG JOBS
BG JOBS
DB

CPU

NODE 4

FG JOBS
BG JOBS
DB

(2)CPU

NODE 2

FG JOBS
BG JOBS
DB

CPU

NODE 3

FG JOBS
BG JOBS
DB

CPU

NIU

NIU LAN 1 NIU

NIU

SYSTEM DATA PROCESSING DEVICE LEGEND

MASS STORAGE

INSTRUMENT

DISPLAY

PROCESSOR   CPU

DPNS VERSION 2.0
SCENARIO 3

NODE 1
FG JOBS
BG JOBS
DB
CPU

NIU

LAN 1

NODE 2
GATEWAY

NODE 3
GATEWAY

NODE 1
FG JOBS
BG JOBS
DB
CPU

NIU

LAN 2

NIU

NODE 2
FG JOBS
BG JOBS
DB
(2)CPU

NODE 3
FG JOBS
BG JOBS
DB
CPU

SYSTEM DATA PROCESSING DEVICE LEGEND

MASS STORAGE		INSTRUMENT
DISPLAY		PROCESSOR CPU

Foreground Job Completion Time (sec)
mean & (sd)

	SCENARIO 1	SCENARIO 2	SCENARIO 3	SCENARIO 3
	1 LAN Localized FG	1 LAN Distributed FG	2 LANs (GW 1 Mbit/sec) Distributed FG	2 LANs (GW .5 Mbit/sec) Distributed FG
Low activity BG	589 (28)	557 (28)	658 (155)	713 (164)
High activity BG	663 (86)	802 (377)		

User Interface

Present: INGRES Data Base on Vax

Testing soon: INGRES Data Base on IBM AT

Planning: Window and graphics environment
on IBM AT

Concept definition: Expert user interface on next
generation personal workstation

Future Development

Respond to user needs

- Scenarios

- Job types

- Devices

Increase the sophistication of
the user interface

- Graphics

- AI technology

Some ideas:

- User defined job(s) (at run-time)

- Library of pre-defined jobs

- ISO/OSI protocols

- Turn into stand-alone system

DISTRIBUTED PROCESSING CONCEPTS

INTRODUCTION

&

FDDI/FODS BASIC COMPARISON

Williamsburg Workshop

November 18-20, 1986

ARC-RI

Terry Grant

DISTRIBUTED PROCESSING CONCEPTS

TECHNOLOGY DEVELOPMENT OBJECTIVES:

Extend Data Processing *Utility* to the End User:

- Increased Performance
- Extensibility
- Availability
- Resourse Management

Importance & Metrics

are Application Dependent

DISTRIBUTED PROCESSING CONCEPTS

METHOD:

   1. BOTTOM-UP UNDERSTANDING...

      NECESSARY FOR NEW SYSTEM INSIGHTS

      COMPONENTS - PROTOCOL - WORKLOAD

      SIMULATION PROVIDES THE PRIMARY BASIS!

   2. TOP-DOWN SYSTEM STUDIES...

      DESIGN EVALUATIONS FOR SPACE STATION

                      FOR AI/AUTOMATION NEEDS

      CONCEPTUAL STUDIES OF DISTRIBUTED PROCESSING

      ANALYSIS - SIMULATION - EMULATION - TEST H/W

       AS REQUIRED (EG.: FOR A NEW DISTRIBUTED OPERATING SYSTEM,
                    FOR RELIABLE DATA NETWORK MANAGEMENT)

   3. DEFINE A DISTRIBUTED PROCESSING RESEARCH FRAMEWORK...

       FOR TRACKING, CHARACTERIZING SIMILAR WORK,

         & PUTTING RESULTS IN THE CONTEXT OF APPLICATIONS

LOAD AND THE LANES3 SIMULATIONS

Load – entered as mathematical distributions.

LOAD – explicitly entered in script.

LAN parametrics

LAN Simulation

FDDI or FODS

WITH COMMON LOAD & BUFFERING

Event Trace

Message by message examination of LAN

Global Results

Station– Specific Results

Ingres Relational Database/Analysis
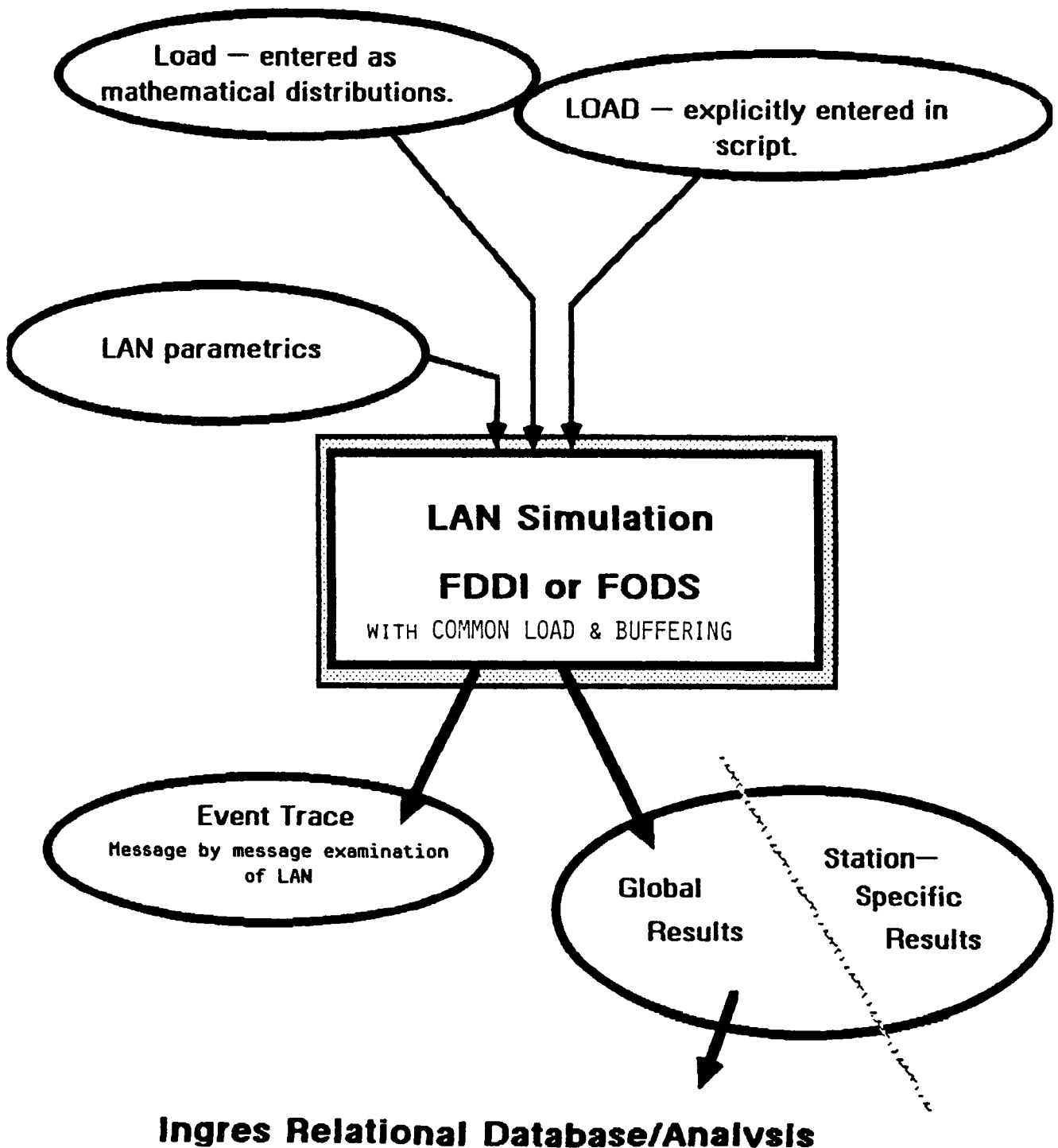
LOCAL AREA NETWORK EXTENSIBLE SIMULATOR

VERSION III

ISO—OSI MODEL
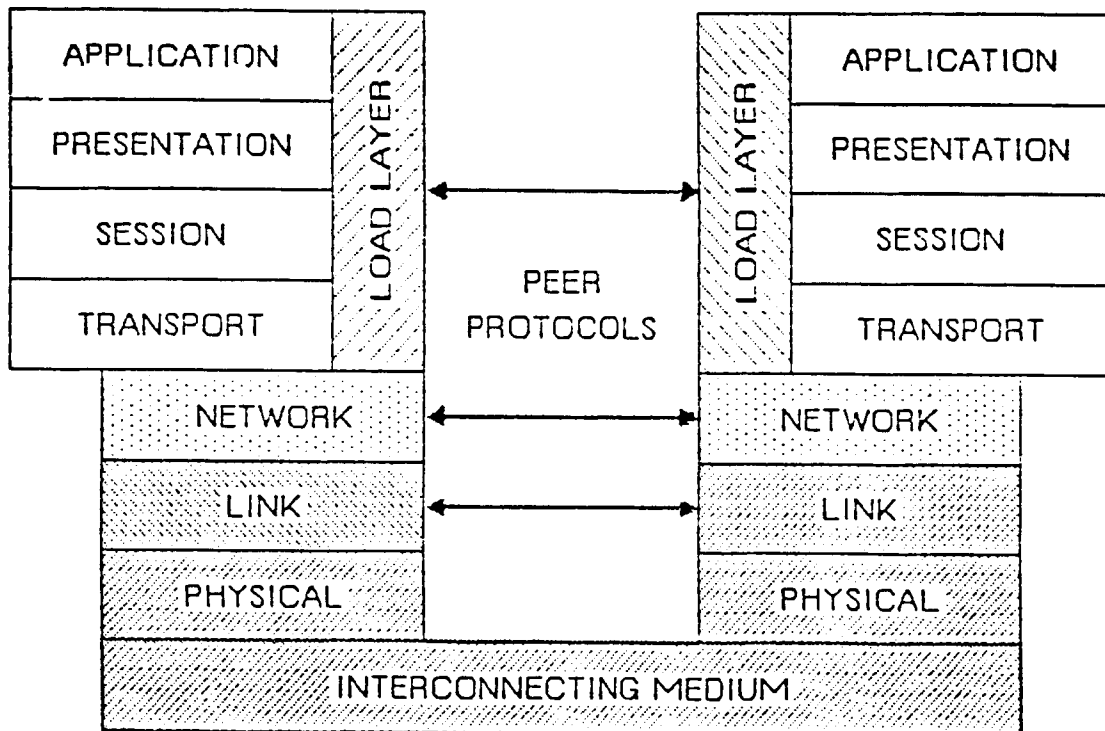
PHYSICAL LAYER	– STAR OR TOKEN PASSING RING
LINK LAYER	– FODS OR FDDI TOKEN RING MEDIA ACCESS CONTROL (ANSI X3T9/84-X3T9.5/883-16 Rev. 7.2)
NETWORK LAYER	– USER DEFINED MESSAGE BUFFERING
LOAD LAYER	– USER DEFINED MESSAGE DESCRIPTORS

PRELIMINARY PERFORMANCE COMPARISON, using LANES3

FDDI(async) vs. STAR*BUS/FODS

ASSUMPTIONS:

- o POISSON DISTRIBUTION on INTER-ARRIVAL of LOAD MESSAGES

- o 2KBYTES PER LINK LAYER FRAME

- o INSTANT RECEPTION OF MESSAGES AT LOAD LAYER (STD ASSUMPTION)

- o LARGE FIFO BUFFERS AT NETWORK LAYER

- o TEN NODES OR STATIONS

BASELINE FOR FUTURE APPLICATION-SPECIFIC STUDIES

AVERAGE LOAD TO LOAD DELAY VS. THROUGHPUT
FODS & FDDI – 10 Stations and Single Frame (2kbyte) Messages

AVERAGE LOAD TO LOAD DELAY VS. THROUGHPUT
FODS & FDDI − 10 Stations and Multiple Frame (2kbyte) Messages
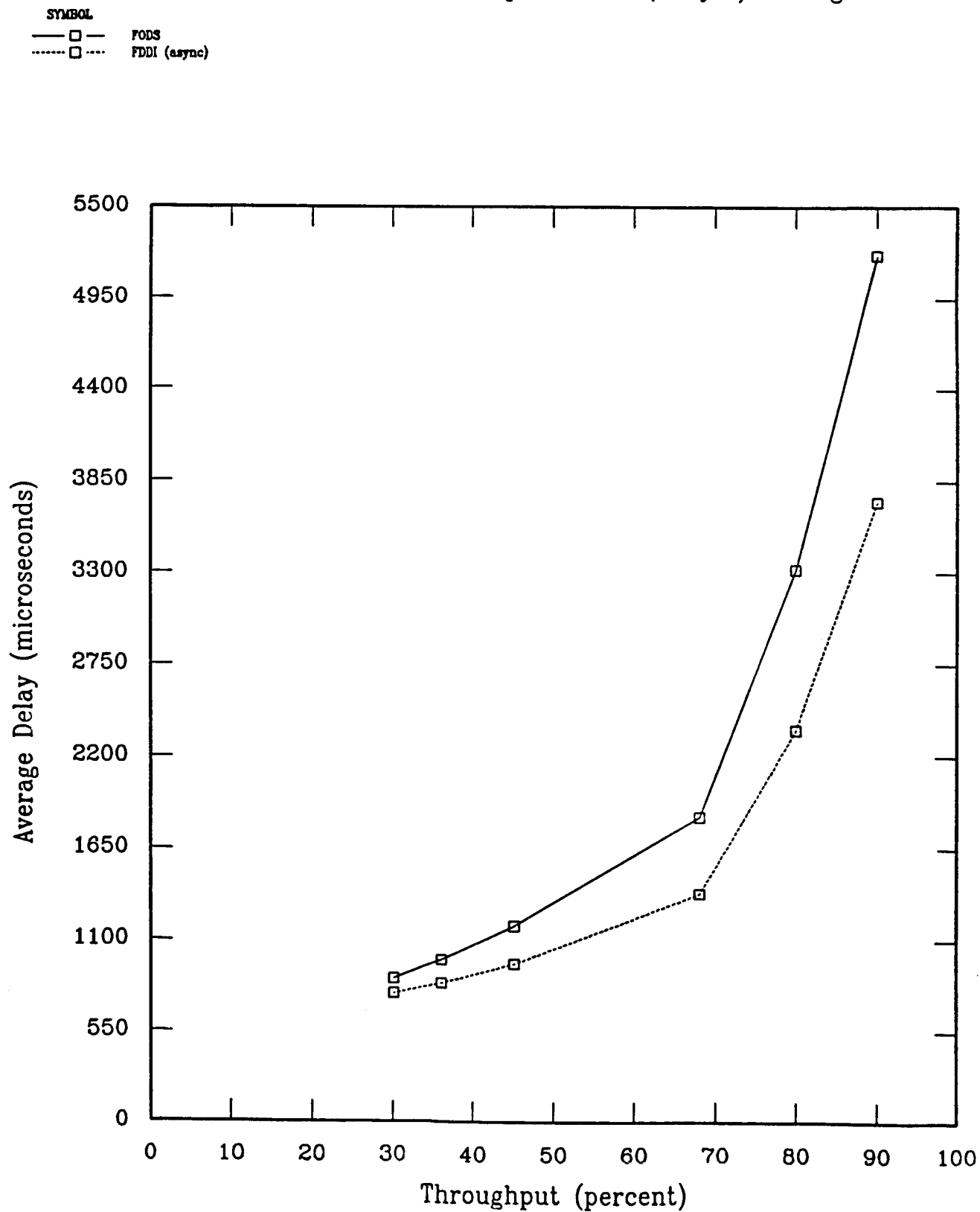
2-138

MAXIMUM LOAD TO LOAD DELAY VS. THROUGHPUT
FODS & FDDI – 10 Stations and Single Frame (2kbyte) Messages

SYMBOL

— □ — FODS
······ □ ···· FDDI (async)
— □ — FODS (average delay)
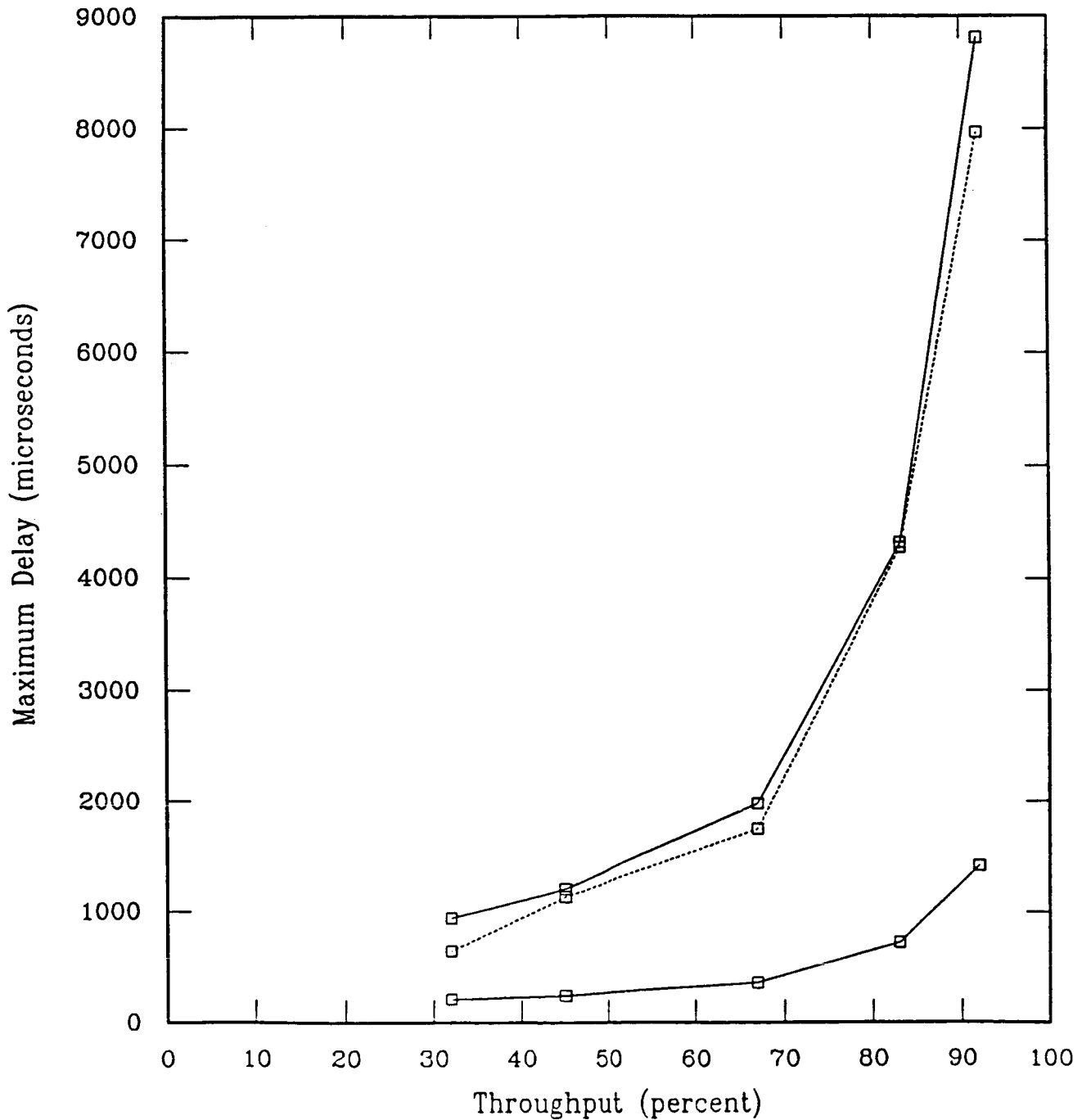
MAXIMUM LOAD-TO-LOAD DELAY DISTRIBUTION
FDDI – 10 Stations and Single Frame (2kbyte) Messages
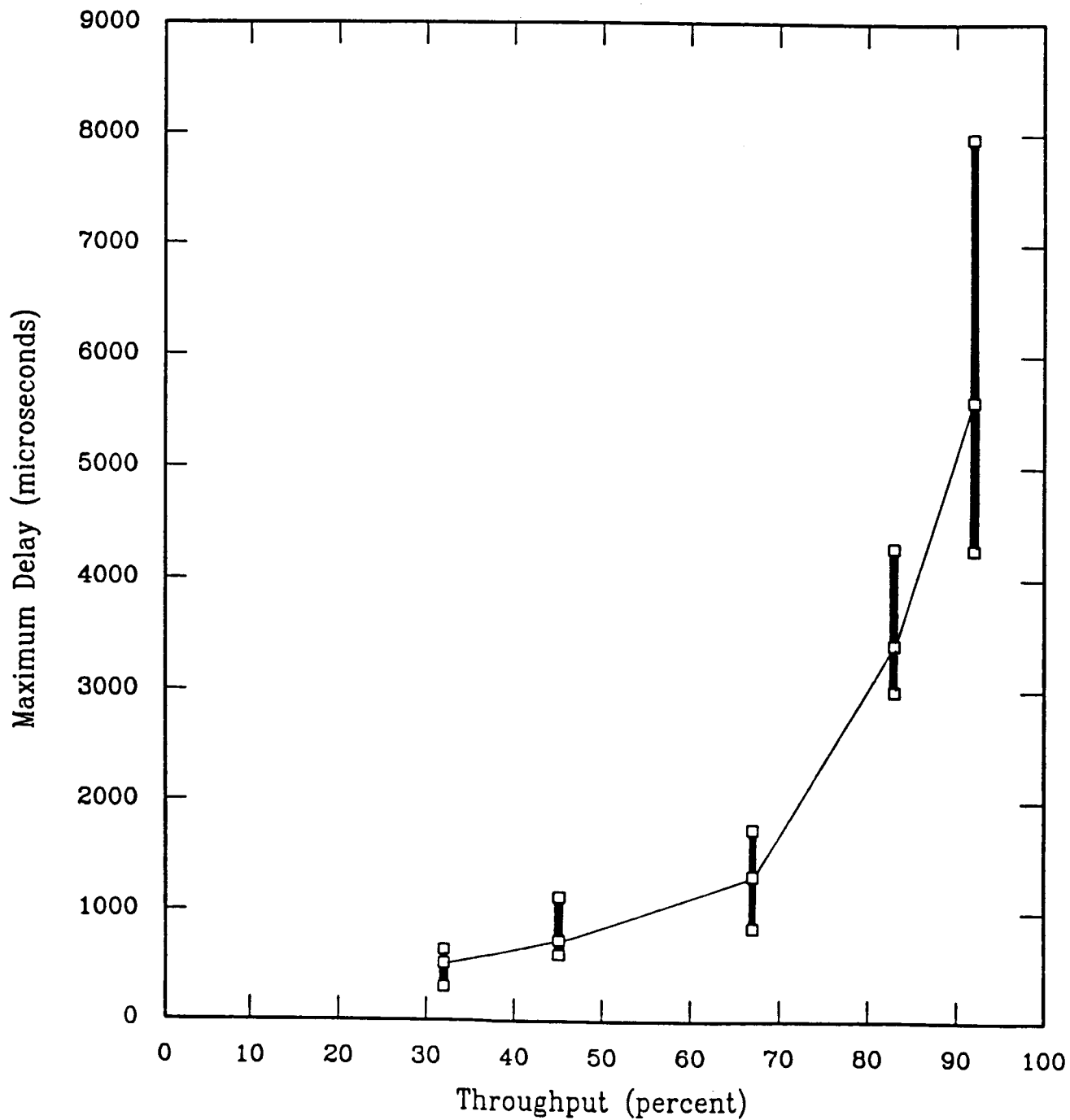
MAXIMUM LOAD-TO-LOAD DELAY DISTRIBUTION
FODS — 10 Stations and Single Frame (2kbyte) Messages
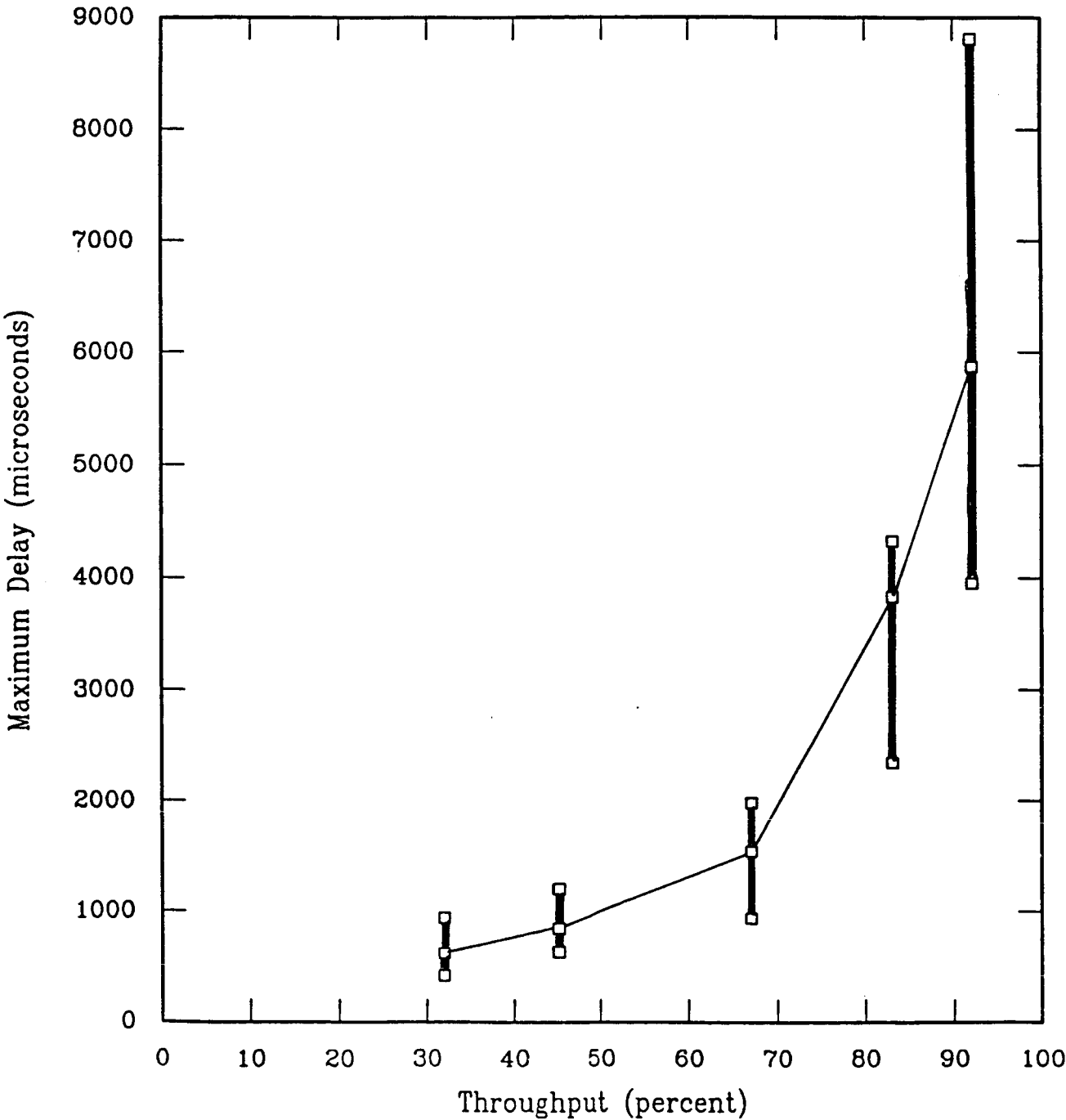
APPLICATIONS INFORMATION AN IMPORTANT NEED

o EXAMPLE - EUROPEAN INDUSTRIAL DATA TRAFFIC MODEL: *

Traffic Scenario	Useful frame length (octets)	Priority	Deadline (ms)	Average number of messages/second/station		
				WORKSHOP	TELEPHONES	FACTORY
ALARMS	30	0	0	1	0	0.25
SENSORS/ ACTUATORS	30	1	5	80	0	20
TELEPHONES	250	1	15	0	32	14,6
TRANSACTIONS	200	2	20	10	0	2
FILES	2000	3	50	0.5	0	0.1

* from Gerard Le Lann, INRIA, France

o SPACE STATION DMS TRAFFIC MODEL(S) ?

o U.S. INDUSTRIAL DATA TRAFFIC MODELS FOR

FDDI, SAE-9B, STAR*BUS ?

A Systems Level Approach
to Distributed Processing

November 18, 1986

by

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A Systems Level Approach to Distributed Processing

Date of Presentation: November 18, 1986

(20:15)

0. (1:30) Introduction
   A. (0:15) [Title] **Title, Name,** and **Extension**
   B. (0:30) [Goal] The overall **project   goal** is to **develop techniques** for **cost-effectively** producing **software** for **high-performance general-purpose** computers.
   C. (0:45) [Presentation] This **presentation** will describe the **problem,** the **necessary elements** of a solution, and an **example** solution.

I. (5:30) [Problem] **Single processor** architectures have hit **physical performance** limits and cannot meet growing needs.

    A. (1:00) [Speed] The **solid** line shows the instruction rate of **high-end commercial** single **processors** versus time. The **dotted** line shows the instruction rates demanded by **high-end commercial applications**. In the past, **memory** speed **was** the **bottleneck**, and only in the **last decade** has a need for **processing** speed been keenly felt. **Today**, commercial high-end **processors are** at or near **fundamental physical limits. Space Station** experiments are **high-end** users.

    B. (1:15) [Communication] Instruction **fetch limitations** are illustrated, by noting that as the **memory** size, indicated by white boxes, **grows, fetch time grows**. The time to **select** a new instruction address at the processor, black box, **address** it, grey box, and **fetch** it, is **bounded** below by signal **propagation** speed. If **memory** elements have a **minimum physical size**, are **accessed** by a **single processor**, with a **random** distribution we can calculate an **upper limit** on **instruction rate. Space Station** experiments will have tight **communication restrictions**.

    C. (0:30) [Miniturization] **Current research** is examining ways to **reduce** the **minimum physical size** of **memory** elements, by using **nonelectronic** storage, such as **optical** or **cryotronic**. These **change** the calculated **performance** limits, but are currently **infeasible**, and only provide a **decade's respite**.

    D. (0:30) [Restructuring] **Current research** is examining ways to automatically **restructure algorithms** to **increase locality**. This also **changes** the calculated **performance** limits, but **typical algorithm** classes, like **compilers** are considered **intractible**.

    E. (0:45) [Parallel] **This** research assumes the use of **parallel processors (black) distributed** through **memory (white)**. As the **tasks** and machine size **grow**, the number of **processors** also **grows**, so **mean communication** distances are **reduced** and **instruction rates increased**.

    F. (1:00) [Saturation] Any **architecture** that imposes **global dependence** on a **fixed set** of components **limits** computer **performance**. When **demand** for the **critical**

component is **low**, the growth in performance is **linear**, dotted line. When the **critical** component is being **fully** utilized, **saturation** is reached as indicated by the **solid** line. When the **critical** component is **overused**, **contention** and other overhead, will frequently **reduce** performance **below saturation**.

II. (6:00) [Solution] We need a computer, with **no** architecturally **imposed** performance **limits.**

A. (1:15) [Extensibility] When we **need more** speed, we need the **ability to add** more **processors** to **increase throughput.** The **dotted** line shows the **ideal growth** of performance with number of **processors.** The **shaded** area indicates the desired **performance** growth when we have **no global dependence** on a **spatially** bound **resource.** For **Space Station, we can't** afford to **swap** out old **hardware** in order to increase performance. For **some** applications, over some finite **range, actual** performance may **exceed** the **ideal** assymptote. **Such** a system is called **extensible** or **scalable.**

B. (1:15) [Dynamic] When physical components **fail,** or task **requirements change,** we need to **switch** component usage **without stopping** the entire machine. The **diagram** shows three **tasks** running on three **subsections** of the machine. When one processor **fails** (**X**), **idling** (**0**) and **replacing** (**circle**) it should **not disturb** the **other** tasks. This means that we have **no global dependence** on a **timely** bound **resource.** In Space Station we can't afford to **shutdown** an entire system to **upgrade** individual subsystems.

C. (0:30) [Reconfigure] **Extensibility + Changeability = Dynamic Reconfigurability.**

D. (1:00) [Classes] These **constraints** can be characterized more **precisely** in terms of **seven constraints** applicable to all levels of **hardware, software,** and **firmware.** A **detailed** explanation of these is **beyond** the **scope** of this talk, but **seven algorithms** can be used to loosely **represent** them. (**Matrix** arithmetic, **Alpha-Beta search, Masking, Tree** sort, **Loader, Exhaustive Graph Tracer, Compiler**)

E. (1:30) [Current] Classic **Vector** (**Kuck**), **Dataflow** (**Gadjski**), and **Neural Net** (**Hopfield**) architectures **can** handle **some** of these algorithms in **parallel,** but not all. In **practice,** any implementation can handle **all** in **sequential** mode, but **not in parallel. Together,** their capabilities **overlap** to form a **complete** set.

III. (7:15) [Example] **Thousands** of processors can be programmed **cost—effectively** by **hierarchically structuring** the **processing** resource similarly to memory.

   A. (1:30) [Multiplier] As a simple **example**, an **eight-byte multiplier** can be built **hierarchically** in **software** from **atomic** processors to obtain a high degree of parallelism. Note that the eight-byte **multiplier recursively** includes four-byte multipliers.

   B. (0:45) [Transparency] The **programmer** using the multiplier **need not know** whether he is using a special-purpose **chip or** a process **structure.** With a **compiler,** the **low-level** details of the machine are **hideable from** the high-level language **programmer.**

   C. (1:00) [Structures] As with data structures, a **small number** of process **structures** suffices. An **example** set is shown, but **applications** and **experience** will **dictate** which particular set among many is most **suitable. If, while,** and **expressions** are the ordinary ones, save that **functions** of **processing** may exist (e.g. run status). **Indirect** addressing **(array brackets)** might simply be **extended** to select **processors** as well as memory. **When** might be used to state an **event,** after which some statement will be executed. Just as memory is requested and freed, processing might be requested and freed with a **halt** statement.

   D. (1:45) [Federal]. A **federal** resource **allocation** scheme is a scalable, **dynamically reconfigurable.** This **walkthru** illustrates a case where process **D requests 2** more resources which are not available until process **B** terminates and **returns** its **6** resources. Note that **successive** levels (G) of the tree control **larger portions** (by factor of 4) of the total resources so that each **node** can see a **constant** service **load.**

   E. (0:45) [Distributed] The **operating system** will be **scalable** if it can run on **any** node. Each **node** must be able to act as a **controller.** Though **remote calls** are **currently** done only on **loosely-coupled** systems, we are discussing a **closely—coupled** system.

   F. (1:00) [Simulation] An **operating system** and several **hardware** implementations have been **designed** and a **register-level simulation** has been performed. The simulation indicated that about **25%** of the processors could be kept usefully **occupied** while **12%** were involved with **overhead.**

IV. (1:00) [Summary] **High performance** requires a scalable, dynamically configurability. This can be **cost-effectively programmed** using **structured progamming** of the **processing** resource and a **dynamically reconfigurable operating system** and **hardware.**

Project Goal

To

Develop Techniques for

Cost Effectively

Programming

High-Performance

General-Purpose

Distributed Processors
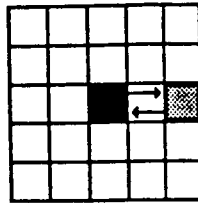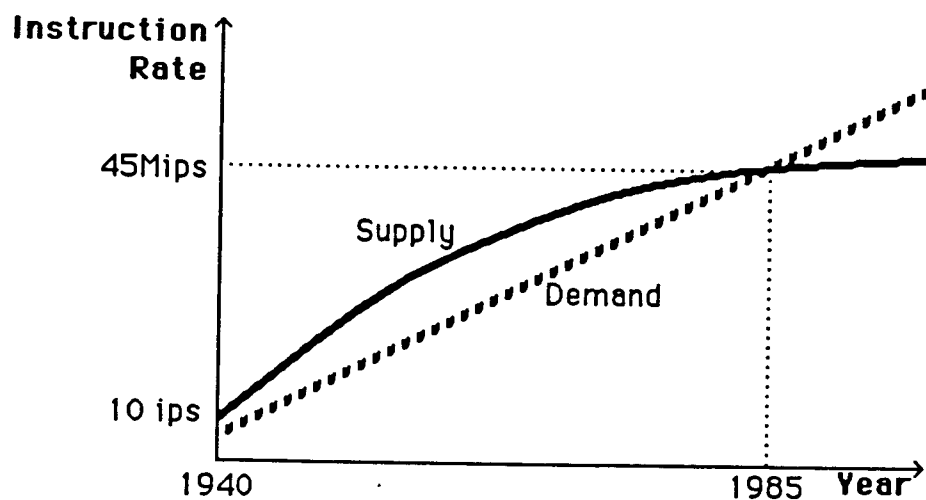
Presentation

Problem

Solution

Example

Problem

Fundamental physical
limits prevent current
computer architectures
from supplying the
processing demands
of the future.

Communication Time versus Memory Size

Processor

Memory

Accessed Memory
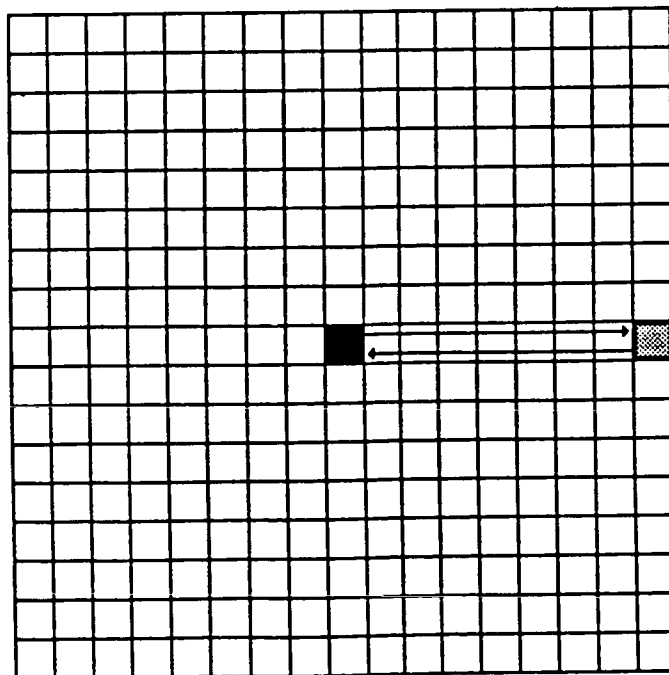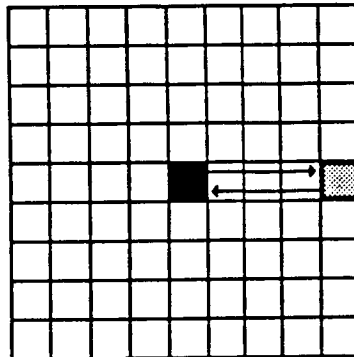
Processing Speed
Supply versus Demand

Current Research to Minimize Physical Size

Josephson Junction
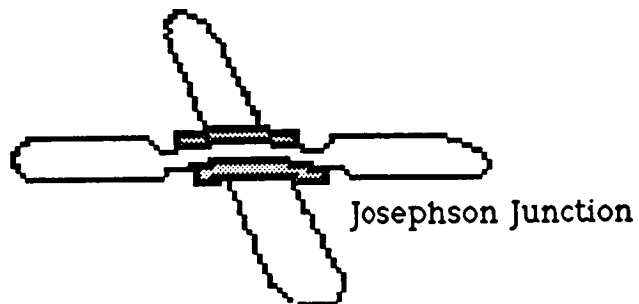
Super-Cooled Memory
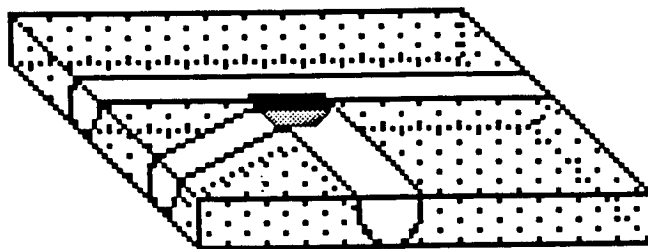
Optical Integration

Current Research to Minimize Access Distribution
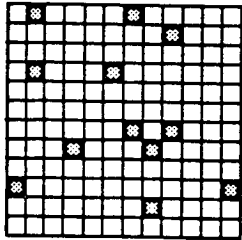
while 0 ≤ i < 11,
 while 0 ≤ j < 11,
  if f(a(i, j)) then
   g(a(i, j))

k = 0
while 0 ≤ i < 11,
 while 0 ≤ j < 11,
  if f(a(i, j)),
   x(k) = a(i, j),
   k = k+1.
 while 0 ≤ l < k
  g(x(k))
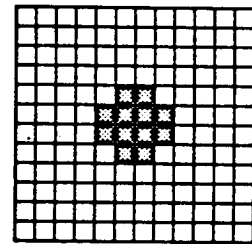
Source Code Restructuring

Communication Time versus Memory Size
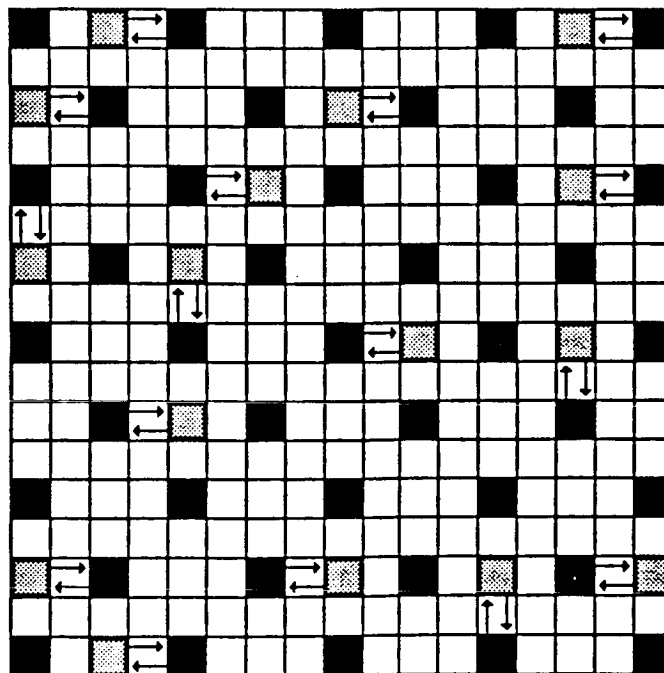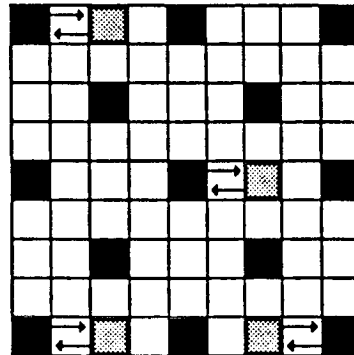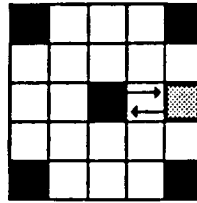
Saturation
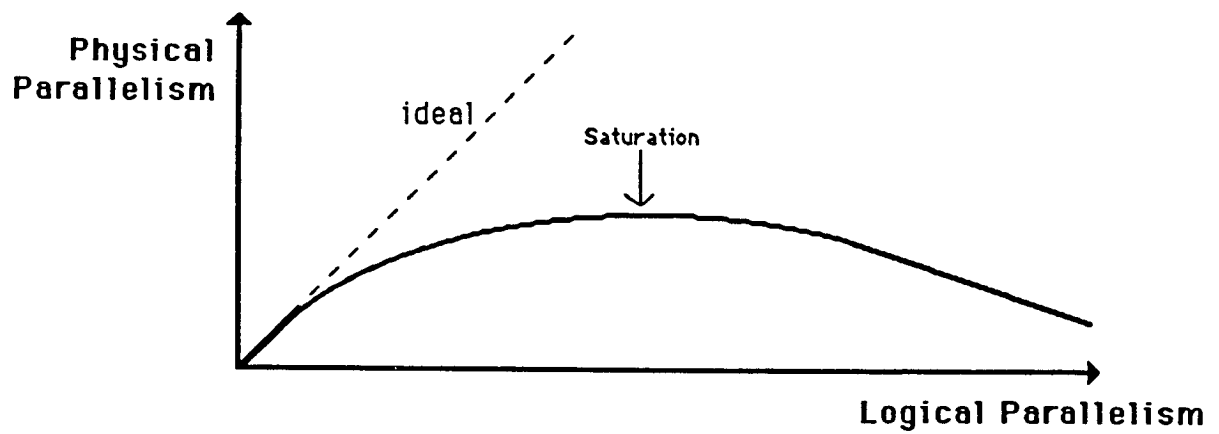
Solution

A scalable,
dynamically
reconfigurable
architecture
is necessary.
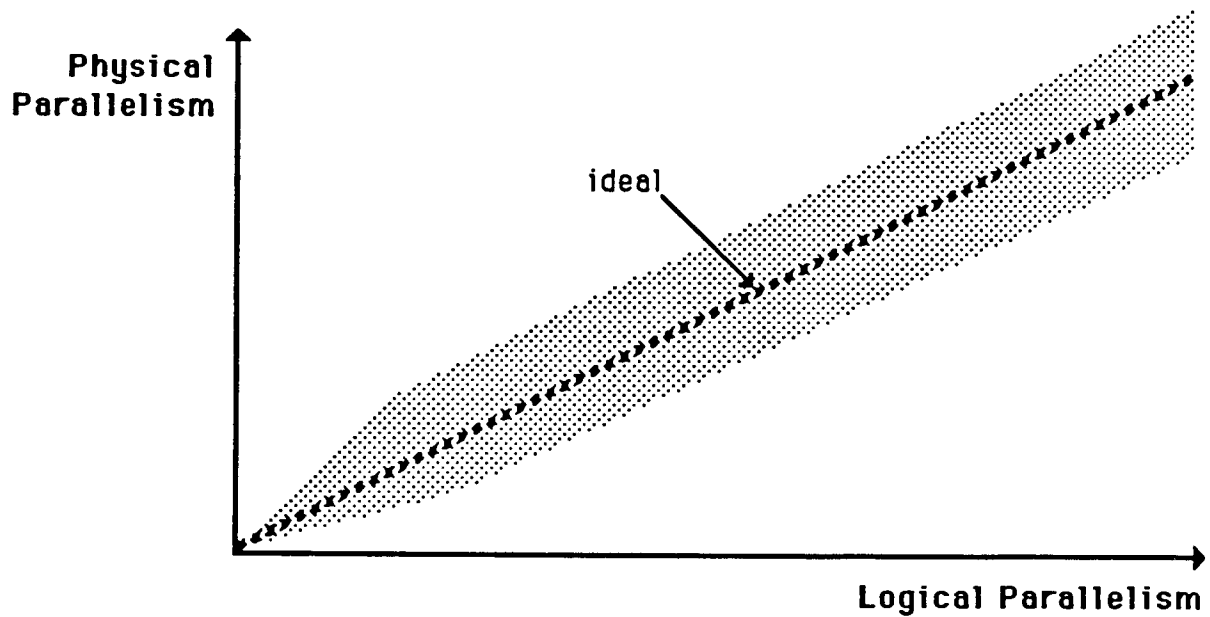
Extensibility

Dynamic Replacement

■ Task 1

▨ Task 2

▨ Task 3

⊠ Malfunctioning
Processor

■ Task 1

□ Task 2

▨ Task 3

◎ Idled
Processor

■ Replacement
Processor
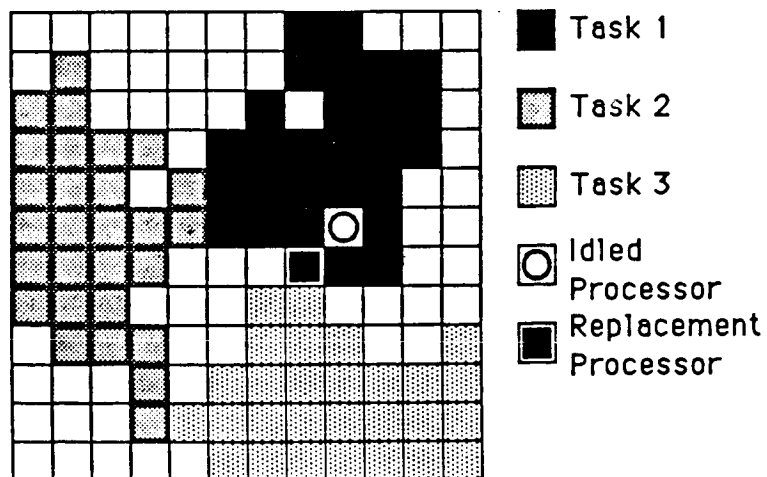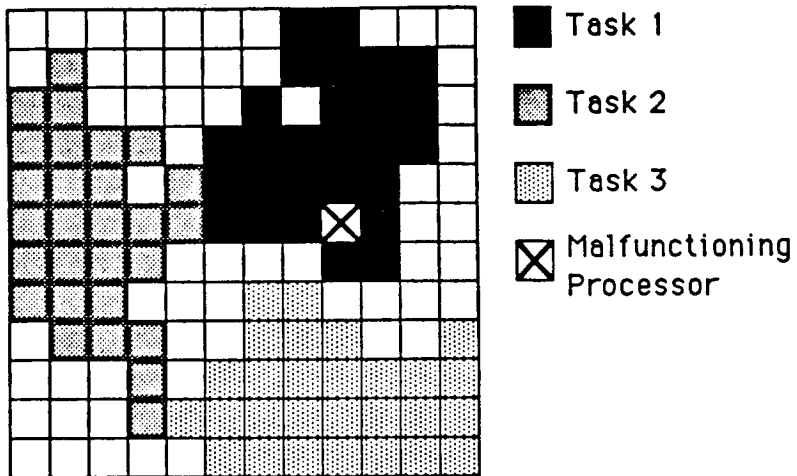
Dynamic Reconfigurability

Extensibility

+

'Hot' Replacement

=

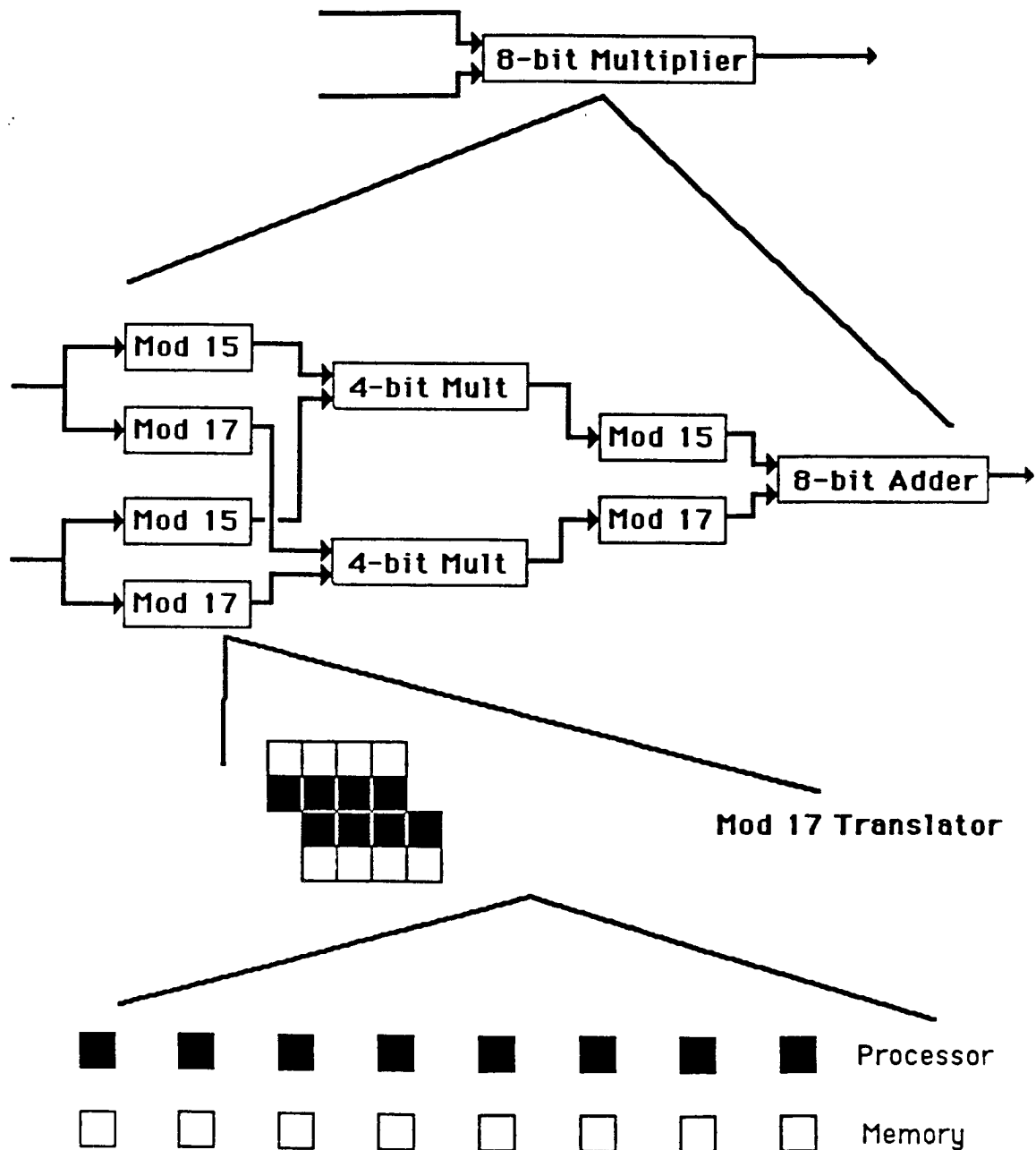# *Dynamic Reconfigurability*

Algorithm Class Representatives

Exhaustive
Graph Tracer

Indirection

Mask

Matrix
Math

Allocation

Compiler
Alpha-
Beta
Search

Condition

Tree Sort

Loader
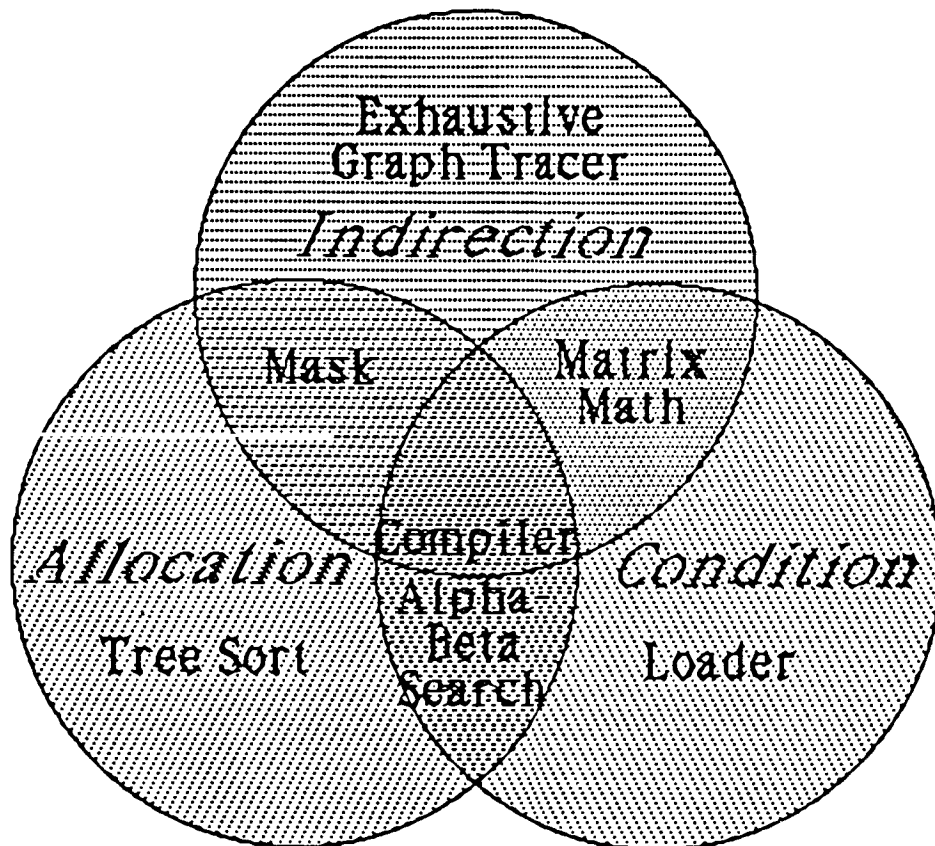
Machine Class
Representatives
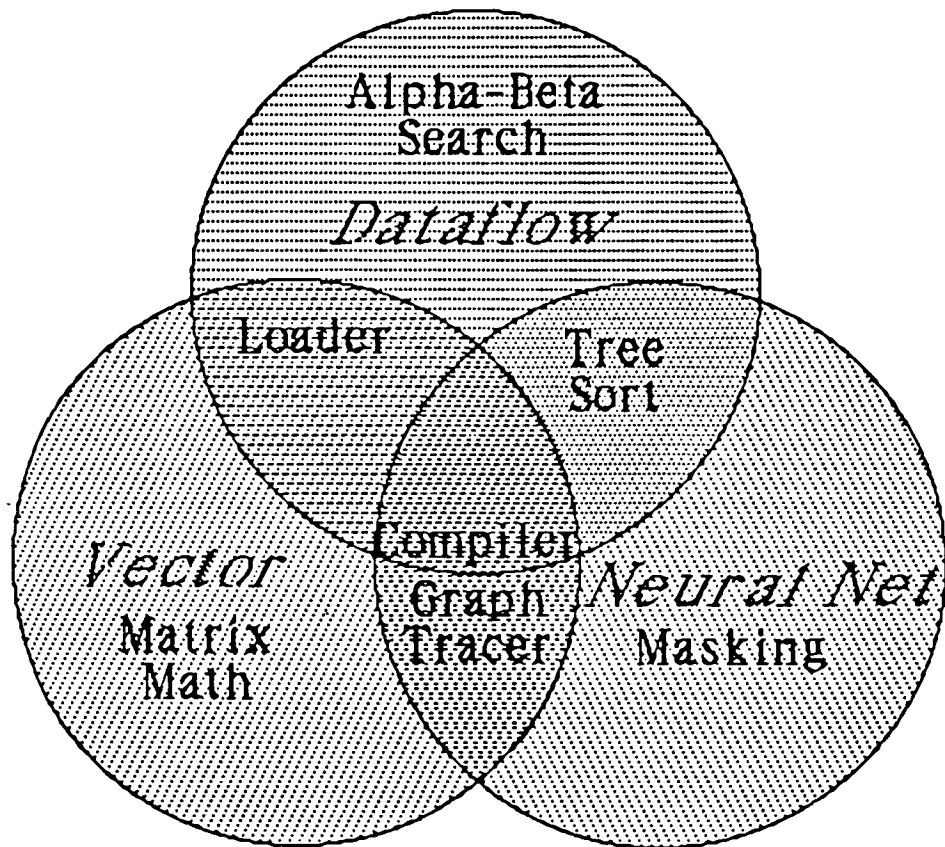
Alpha-Beta
Search

Dataflow

Loader   Tree
            Sort

Vector   *Neural Net*

Compiler
Matrix   Graph   Masking
Math   Tracer

Example

Thousands of
processors can be
cost-effectively
programmed by
structuring the
processing resource
similarly to memory.

# Structured Programming
# of Processing Example

8-bit Multiplier

Mod 15
Mod 17
4-bit Mult
Mod 15
Mod 17
Mod 15
4-bit Mult
Mod 17
8-bit Adder

Mod 17 Translator

Processor

Memory

Compiler Hides Structure versus Special-Purpose Hardware from Programmer

◆ Idle Processor

■ Active Processor

▦ Special-Purpose Hardware

☐ Idle Memory

■ Active Memory
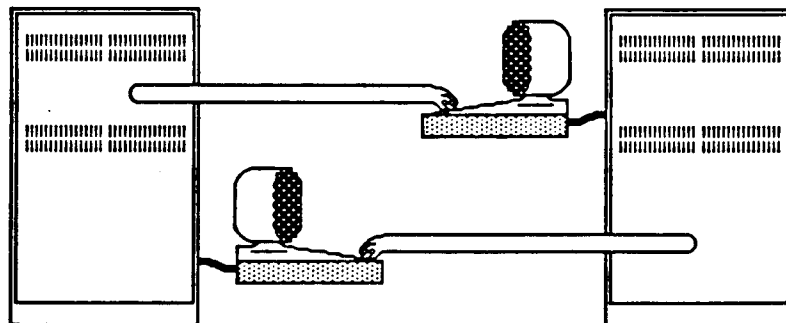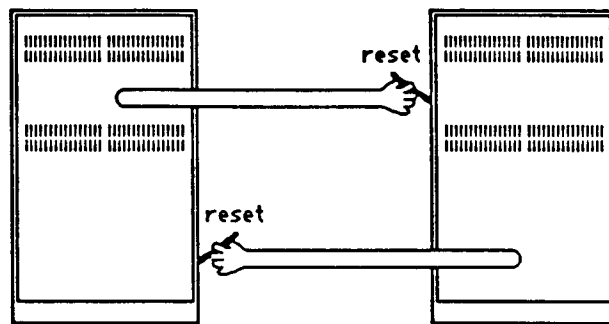
$X*Y \Longrightarrow$ Compiler $\Longrightarrow$

Special-Purpose Hardware

$X*Y \Longrightarrow$ Compiler $\Longrightarrow$

Processing Structure
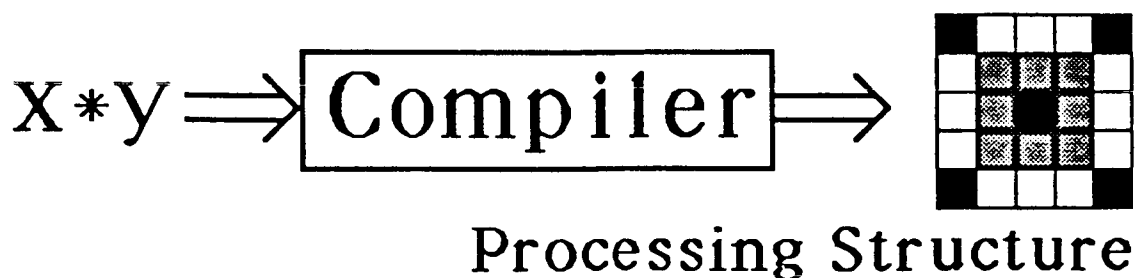
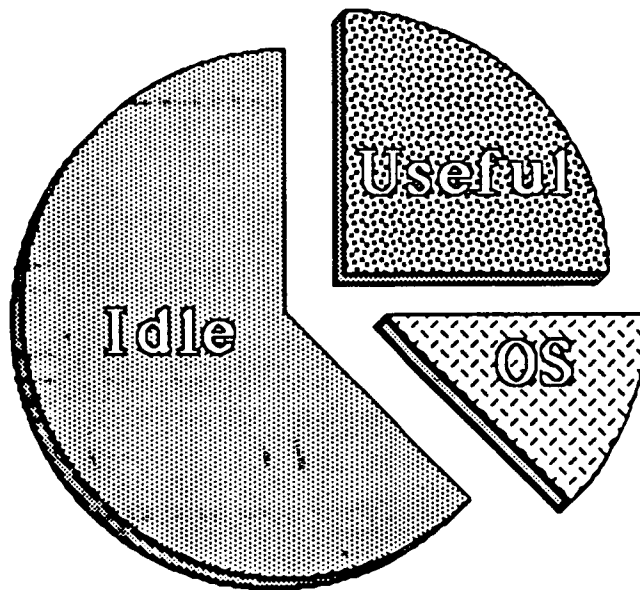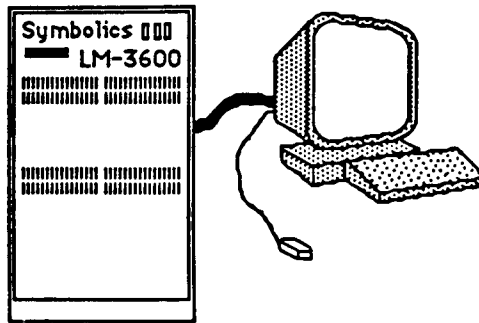# Minimum Processing
Structure Set Example
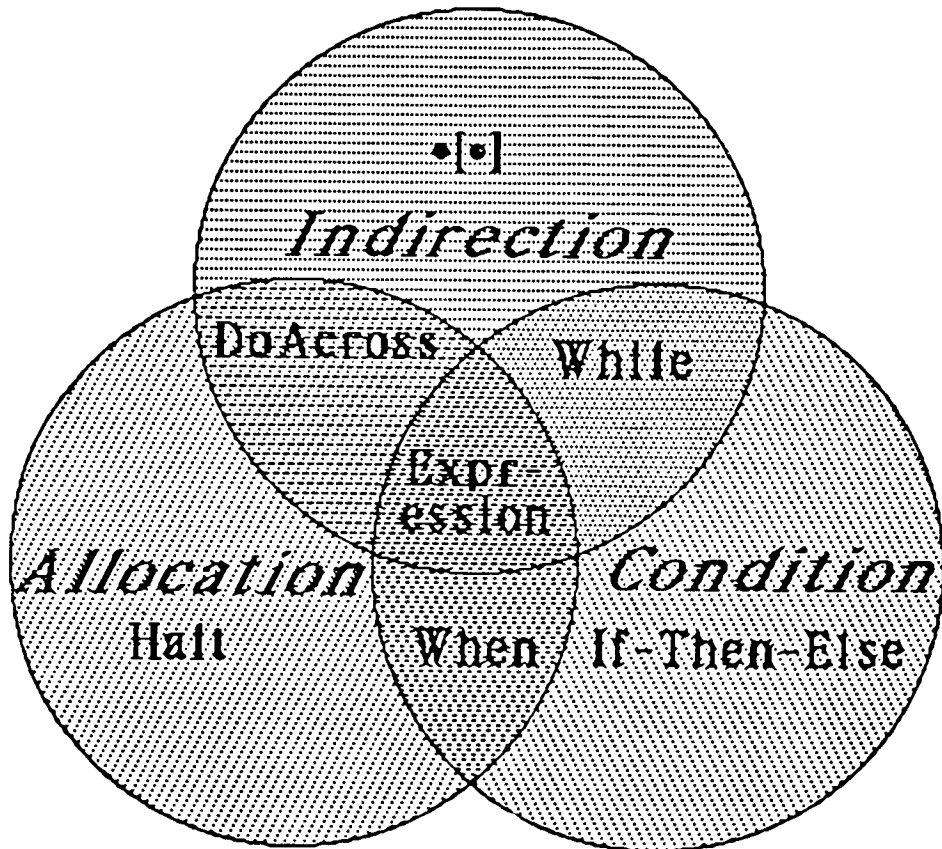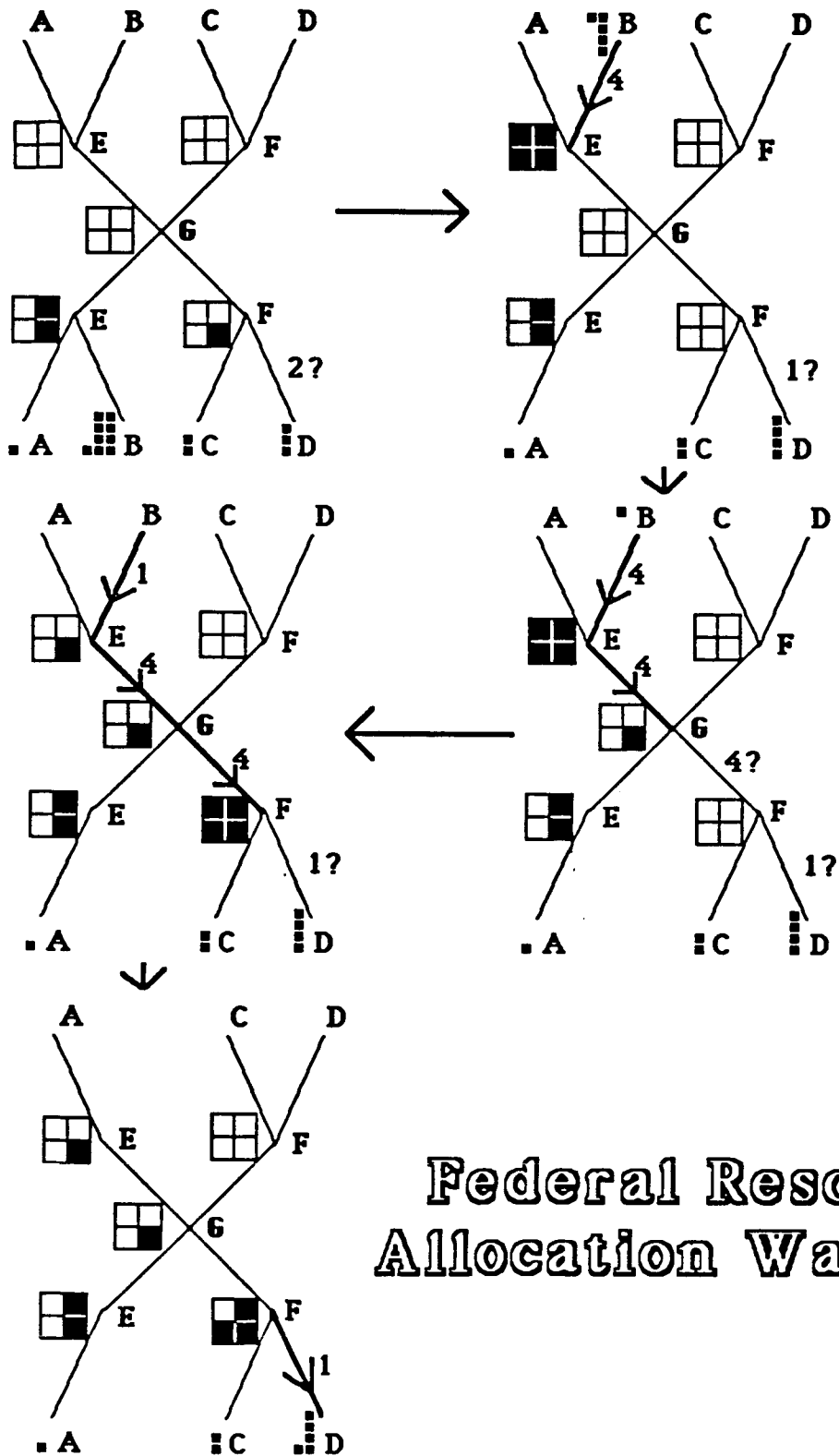
Federal Resource
Allocation Walkthru

Distributed Control

Simulation

Summary

Problem: Fundamental physical
limits prevent current
computer architectures
from meeting the
processing demands of
the future.

Solution: A scalable, dynamically
reconfigurable
architecture is necessary.

Example: Thousands of processors
can be cost-effectively
programmed by
structuring the
processing resource
similarly to memory.

SPACEBORNE OPTICAL DISK
CONTROLLER DEVELOPMENT

Thomas A. Shull

National Aeronautics and Space Administration

Langley Research Center, Hampton, Virginia

PERFORMANCE GOALS

Capacity .... 10^{12} Bits

Data Rate .... 1.6×10^9 Bits/s

Read Error Rate .... $< 10^{-12}$

Data Access Time .... < 0.1s

1.0m

1.0m

0.8m

SHAFT

DISK 1

COLLAR ASSEMBLY
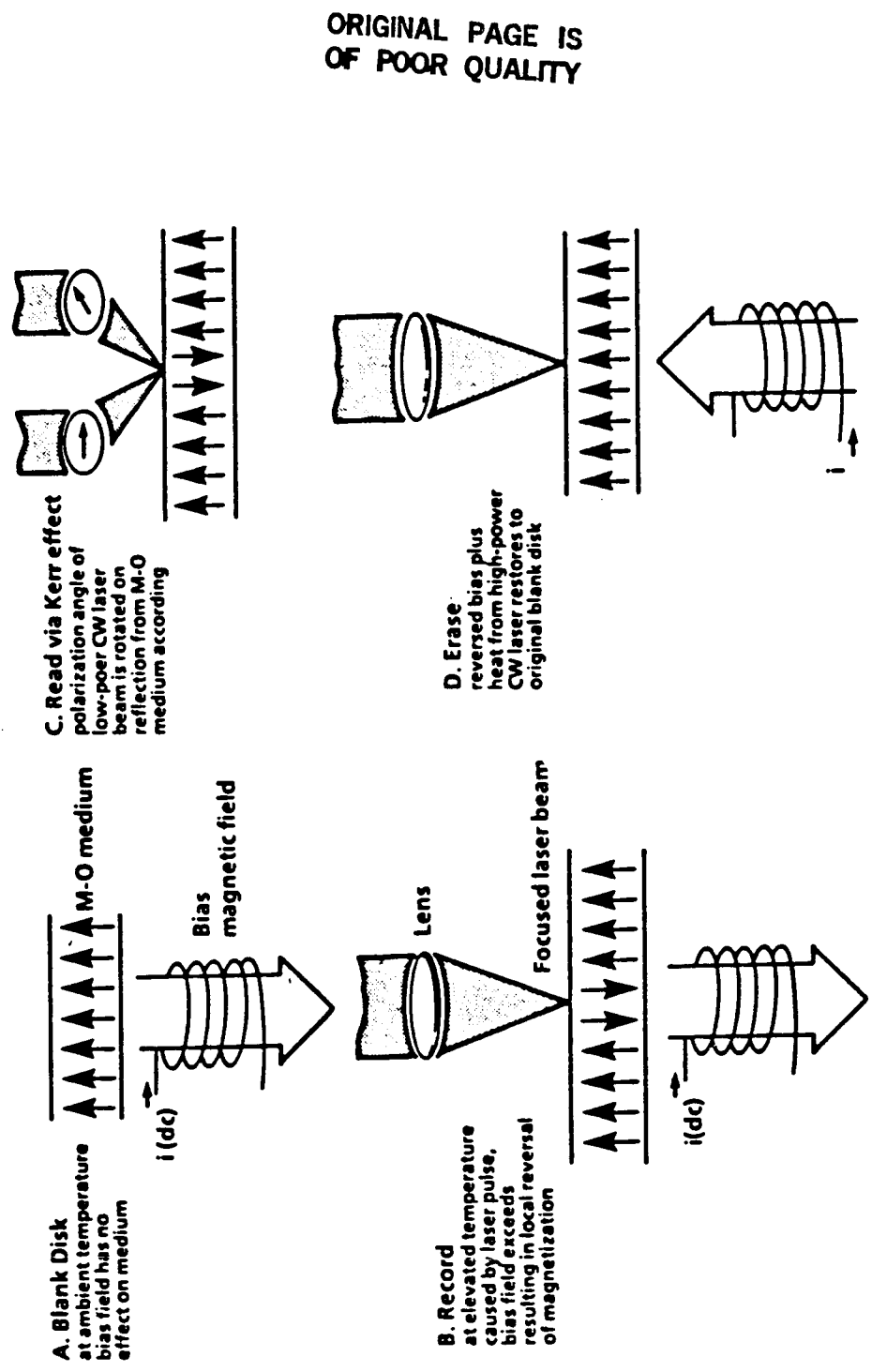
OPTICAL MODULE
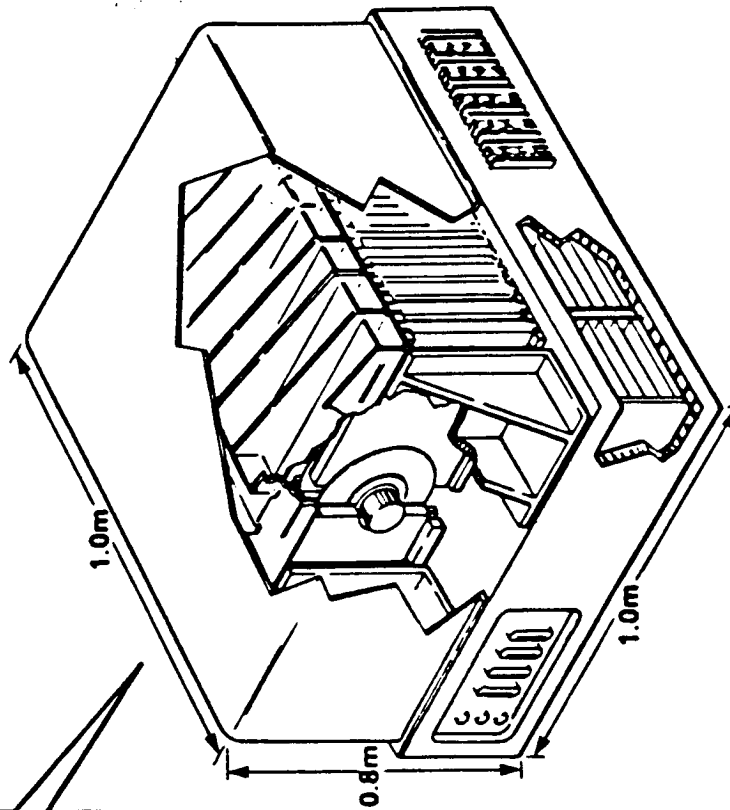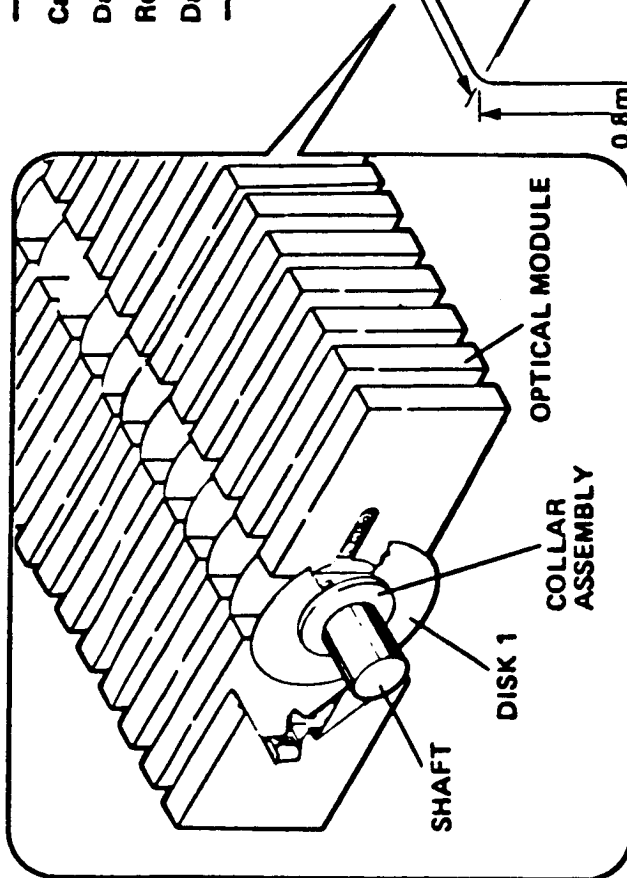
FEATURES

- Erasable, Reusable Media
- 14 - inch Disks
- 24 Surfaces
- 24 Optical Heads
- Solid-State Lasers
- 9-Diode Arrays
  - 8 Data Tracks
  - 1 Pilot Track

Optical Disk Buffer / Preliminary Design Review

Magneto-Optic Recording Process

A. Blank Disk
at ambient temperature
bias field has no
effect on medium

M-O medium

Bias
magnetic field

i (dc)

B. Record
at elevated temperature
caused by laser pulse,
bias field exceeds
resulting in local reversal
of magnetization

Lens

Focused laser beam

i(dc)

C. Read via Kerr effect
polarization angle of
low-poer CW laser
beam is rotated on
reflection from M-O
medium according

D. Erase
reversed bias plus
heat from high-power
CW laser restores to
original blank disk

i

Optical Disk Buffer / *Preliminary Design Review*

SPOT GEOMETRY AND TRACK SPACING

DATA BAND

20 μm

1.4 μm

PERMANENT PILOT TRACK

- GEOMETRY
  - 9 ELEMENT ARRAY — 8 DATA + 1 TRACKER
  - 1.4 μm TRACK PITCH
  - 2.1 μm GUARD BAND BETWEEN DATA BANDS
  - 0.7 μm SPOT DIAMETER
- TRACKING
  - SPIRAL PATTERN
  - CLOSED LOOP RECORDING AND PLAYBACK
  - PREFORMATTED PERMANENT PILOT TRACK
  - PILOT TRACK CONTAINS RADIUS (TRACK NUMBER) IDENTIFICATION DATA AT SEPARABLE LOW DATA RATE
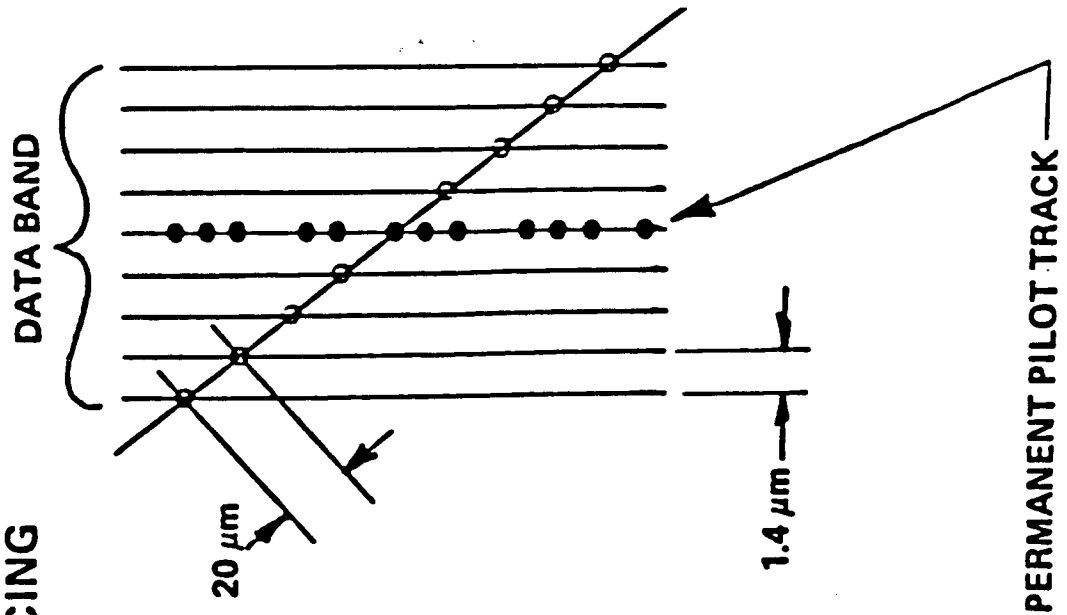
Optical Disk Buffer

BUFFER DATA TRACK SPECIFICATION

NUMBER OF USER BITS/REVOLUTION/TRACK	1,081,344
NUMBER OF FORMATTED BITS/REVOLUTION/TRACK	1,297,612.8
OVERHEAD ADJUSTMENT FACTOR (1)	1.20
NUMBER OF SECTORS/REVOLUTION/TRACK	33
NUMBER OF USER BITS/SECTOR	32,768 BITS
MINIMUM RECORDING RADIUS	4.330 INCHES
MAXIMUM RECORDING RADIUS	6.805 INCHES
TOTAL RECORDING DISTANCE	2.475 INCHES
RECORDING SPOT SIZE	0.71 μM
RECORDING DENSITY [3 $\varnothing$ (1,7) CODE]	0.75 FEATURES/BIT
TRACK DENSITY	8 TRACKS/13.3 μM
NUMBER OF TRACKS/SURFACE	37,813
TOTAL BUFFER USER DATA CAPACITY (24 SURFACES)	9.813×10^{11} BITS
DISK ROTATION RATE	15.413 R/S
USER DATA RATE	16.67 MB/S
FORMATTED DATA RATE	20.00 MB/S

(1) THE DATA OVERHEAD FACTOR FOR THE PROTOTYPE WILL BE 20%. THE BRASSBOARD WILL NOT USE ALL THE OVERHEAD CONTRIBUTORS (E.G. EDAC) OF THE FINAL SYSTEM, BUT THE FORMATTED RATE OF THE FINAL SYSTEM WILL BE MAINTAINED. THUS, THE DATA STREAMS FROM THE BRASSBOARD BUFFER WILL BE DISCONTINUOUS.

3-3

SPACEFLIGHT OPTICAL DISK CONTROLLER DEVELOPMENT
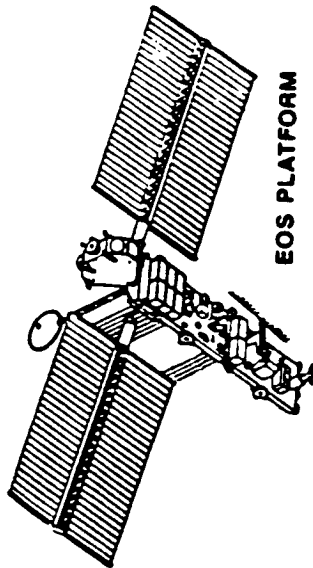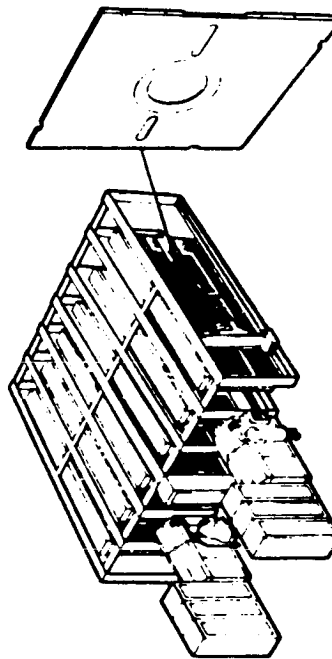
OBJECTIVES

Foster the application of Erasable Optical Disk Memory Technology for NASA Space-flight Data Systems, with emphasis on developing system controller designs which meet NASA mission requirements and constraints.

□ Develop and maintain technical cognizance of the Optical Disk Buffer develop-ment and ground controller development

□ Review the Optical Disk Buffer design as it evolves for areas potentially affect-ing spaceflight utilization and NASA unique requirements and constraints

□ Provide an advocacy support role for implementation of this technology into NASA spaceflight applications

□ Develop NASA system-level user interface functional requirements for space-flight applications

□ Translate system-level requirements into controller interface requirements

□ Develop a flight controller system; which, combined with the Optical Disk Buffer will provide a key capability for future spaceflight data and information systems

APPLICATION DRIVERS

EOS PLATFORM

SPACEBORNE

MULTIPLE HOST/SOURCE

LAUNCH SURVIVAL

SPACE ENVIRONMENT

DIVERSITY OF DATA ROUTES

GROUND BASED

HIGH SPEED MASS MEMORY

DATA ARCHIVES

CONTROLLED ENVIRONMENT

NETWORK/BUS INTERFACE

POTENTIAL APPLICATION
OF AN
OPTICAL DISK MASS
MEMORY SYSTEM
(ODMMS)

TDRSS .

300 MBPS

ODB

EOS PLATFORM

160 MBPS

300 MBPS

2 MBPS

HIRIS

MODIS

SAR
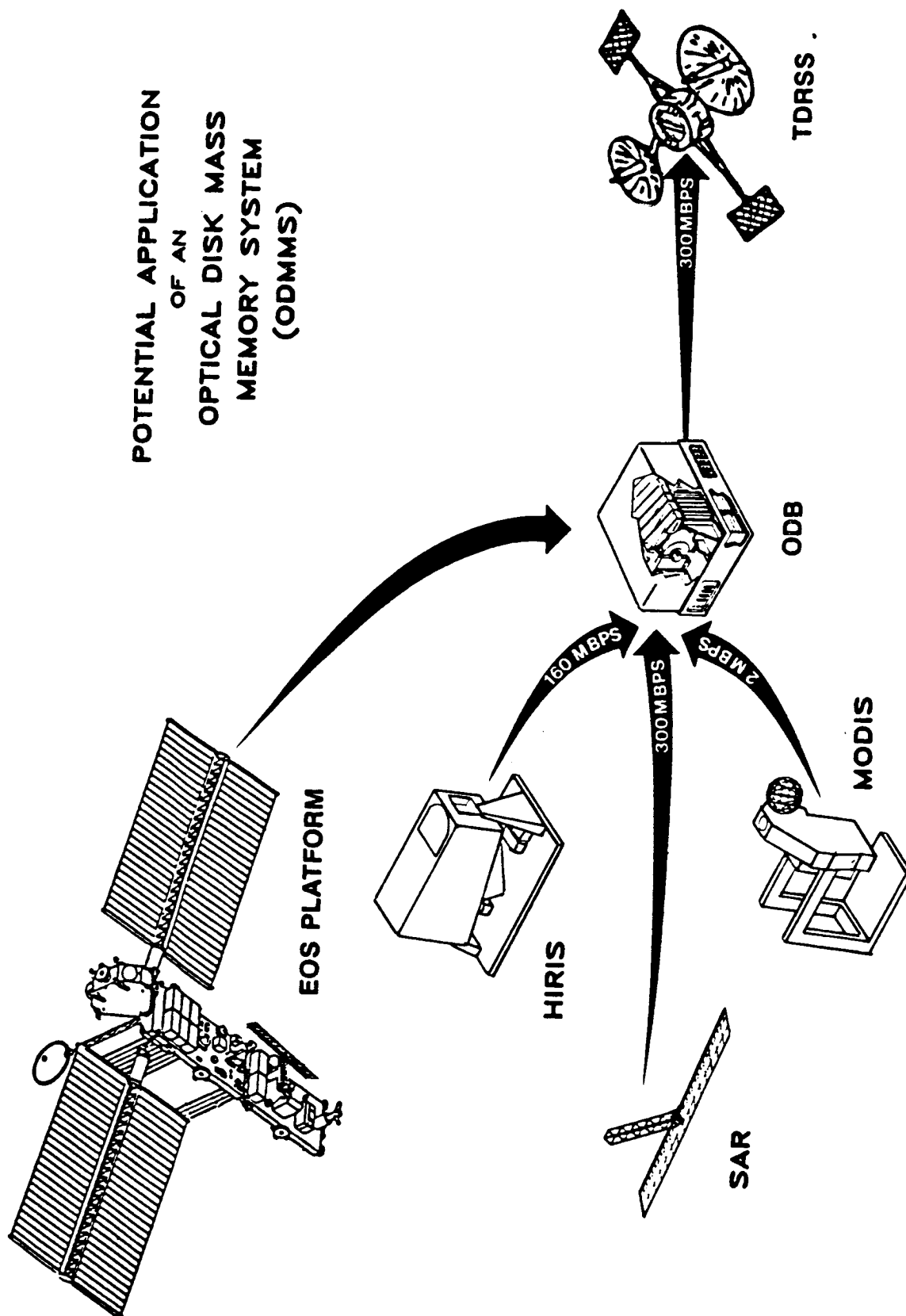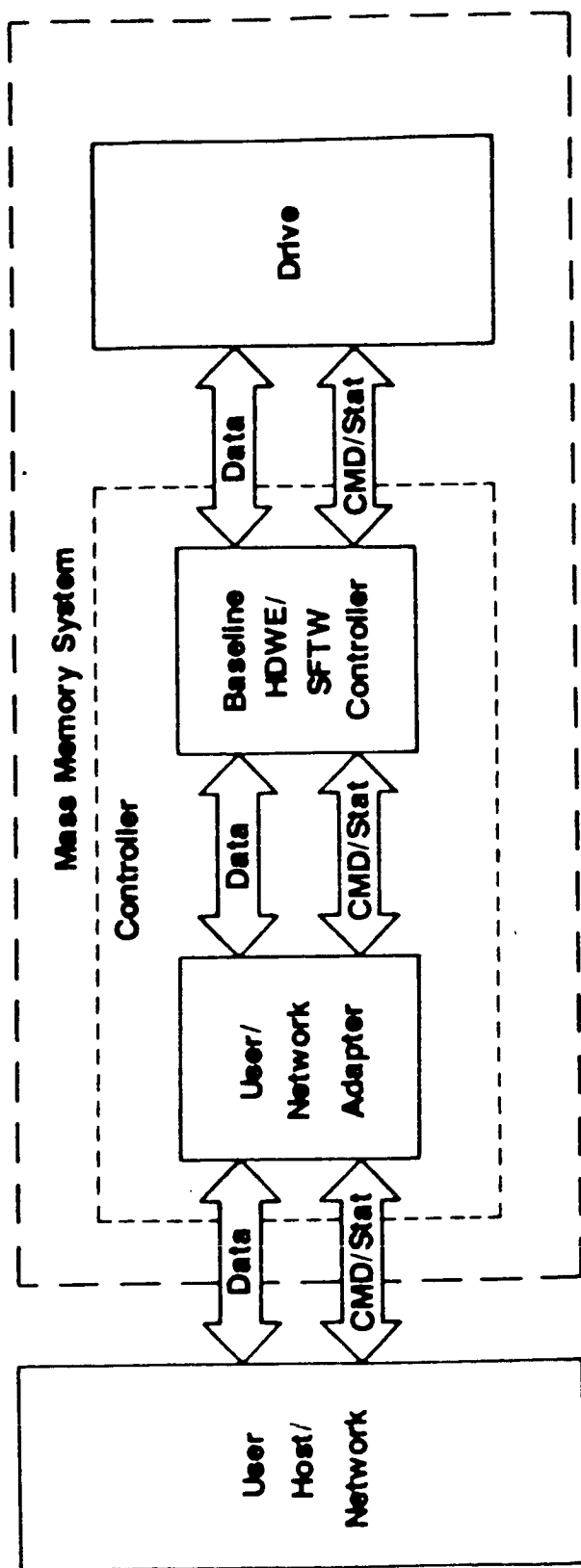
TOP LEVEL ARCHITECTURE

FOR

OPTICAL DISK MASS MEMORY SYSTEM

TAS 8/86

2-181

ODMMS INTERFACE/SYSTEM CONSIDERATIONS

SYSTEM TOPOLOGY

MULTIPLE USER   SINGLE USER/HOST   NETWORK RESOURCE
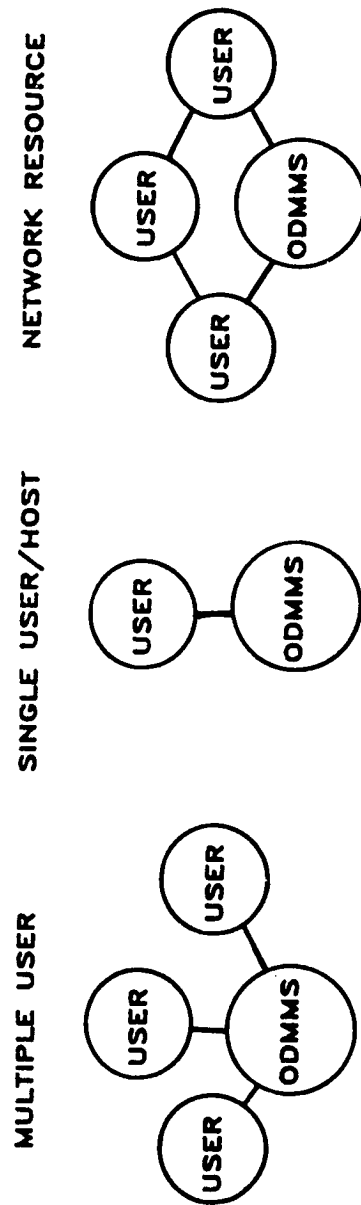
STORAGE APPLICATION

RANDOM ACCESS MEMORY (NON SEQUENCIAL FILES)

FIFO BUFFER (TEMPORARY STORAGE WITH I/O RATE CHANGE)

SPOOLER (LONG CONTINUOUS FILES)

SPACEBORNE ODMMS

OPERATIONAL AND ENVIRONMENTAL CONSIDERATIONS

DATA RATE AND CAPACITY

SELF TEST

DYNAMIC RECONFIGURATION

MODULARITY

SERVICEABILITY

SIZE, WEIGHT AND POWER

LAUNCH SURVIVAL

VACUUM

ZERO GRAVITY

RADIATION

ANGULAR MOMENTUM (DRIVE)

TAS 8/86

FUNCTIONAL PARTITIONING ISSUES

ERROR CORRECTION/DETECTION (EDAC)

DATA FORMATTING

DATA MULTIPLEXING

FILE MANAGEMENT

READ/WRITE DATA BUFFERS

SELF TEST/DIAGNOSTICS

CONFIGURATION CONTROL

OPERATIONAL REQUIREMENT DRIVERS

DYNAMIC RECONFIGURATION

I/O RATE CHANGE

SIMULTANEOUS INPUT AND OUTPUT

USER FUNCTIONAL/PHYSICAL INTERFACE

FUTURE WORK

OPTICAL DISK BUFFER

TECHNOLOGY DEMONSTRATION 1987

BRASSBOARD ODB DEMONSTRATION — 1987

ODB ENGINEERING DEMONSTRATION UNIT

CONTROLLER
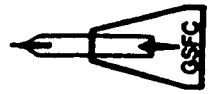
SPACEBORNE ODMMS/CONTROLLER REQUIREMENTS DOCUMENT

CONTROLLER-TO-DRIVE INTERFACE DEFINITION STUDY

CONTROLLER CONCEPTUAL DESIGN

BRASSBOARD CONTROLLER

BRASSBOARD CONTROLLER/ODB ENGINEERING DEMO UNIT
INTEGRATION AND TEST

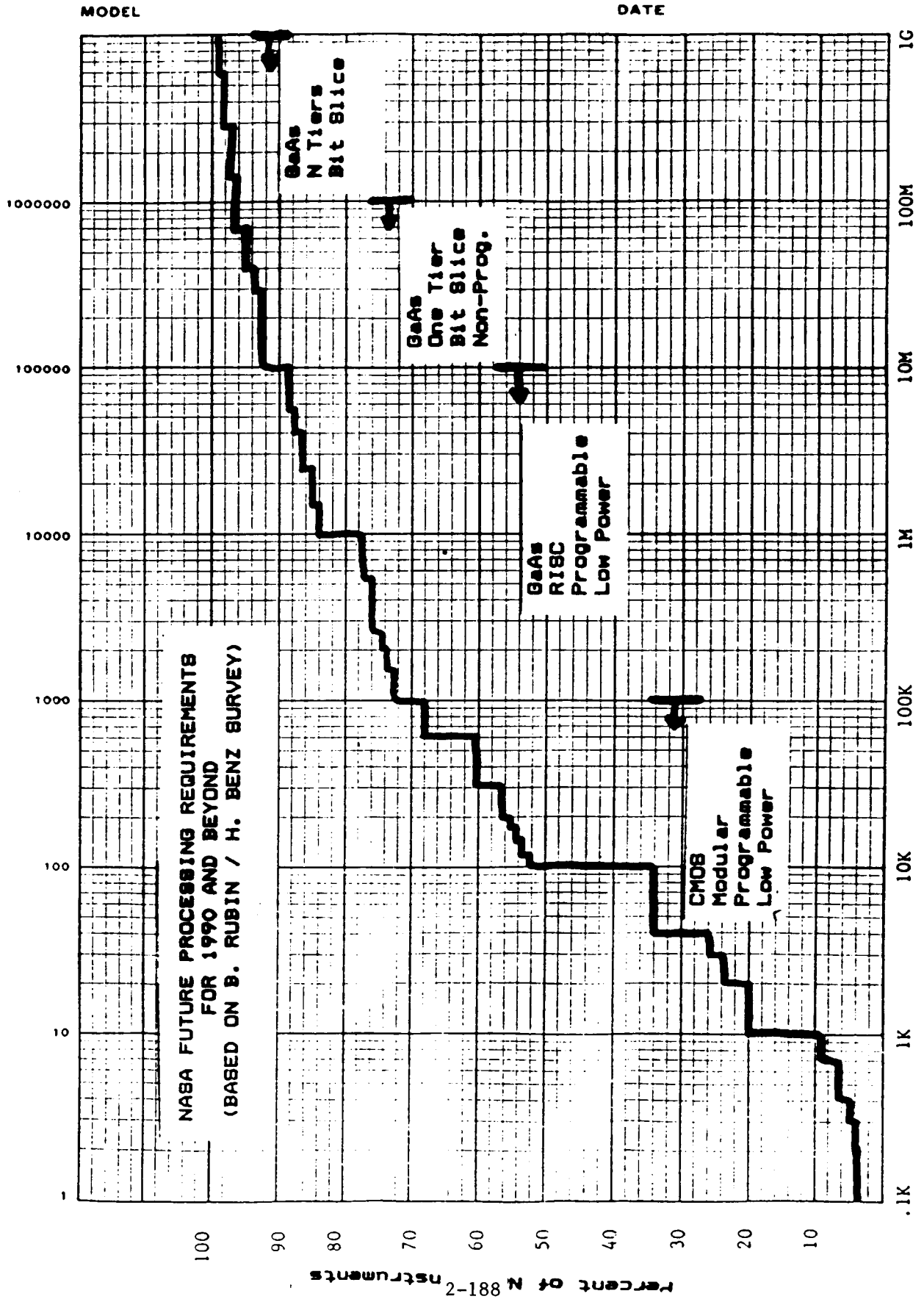ON-BOARD GAAS PROCESSOR DEVELOPMENT

GSFC

GAAS PROCESSOR DEVELOPMENT

- PROGRAM OBJECTIVES

  - TO ADVANCE THE STATE-OF-THE-ART IN ONBOARD HIGH DATA RATE SIGNAL PROCESSING AND STORAGE APPLICATIONS

  - TO DEVELOP A GAAS CHIP SET CAPABLE OF

    - HIGH LEVEL RADIATION TOLERANCE

    - LOW POWER

    - VERY HIGH DATA RATE THROUGHPUT (1000-3000 MIPS)

    - ADAPTABLE ARCHITECTURE

  - TO DEVELOP ADVANCED COMPUTER ARCHITECTURES

MODEL

DATE

GaAs
N Tiers
Bit Slice

GaAs
One Tier
Bit Slice
Non-Prog.

GaAs
RISC
Programmable
Low Power

NASA FUTURE PROCESSING REQUIREMENTS
FOR 1990 AND BEYOND
(BASED ON B. RUBIN / H. BENZ SURVEY)

CMOS
Modular
Programmable
Low Power

Instrument Real Time Data Rate (bps)

Percent of N Instruments

GAAS PROCESSOR DEVELOPMENT

SEMICONDUCTOR TECHNOLOGY COMPARISONS
(ANALYSIS USING 1 MICRON TECHNOLOGY)

TECHNOLOGY	SPEED (PSEC)	TEMPERATURE RANGE	TOTAL DOSE (RADS)	DOSE RATE (RADS/SEC)	COMPLEXITY (EQ. GATES)
CMOS	300	-40C - +125C	10**6	3x10**9	200K
ECL	130	0C - +85C	10**6	10**9	10K
GAAS MESFET:					
D MODE	30	-200C - +200C	10**8	10**10	8K
E/D MODE	20	-200C - +200C	10**8	10**10	4K
GAAS HEMT	12	-200C - +200C	10**8	10**10	2K
GAAS HBT	30	-200C - +200C	10**8	10**10	200

GAAS PROCESSOR DEVELOPMENT

- APPROACH

  - DEVELOP AN ADAPTIVE PROGRAMMABLE PROCESSOR (APP) CHIP SET

    - STRUCTURE AROUND 8-BIT SLICE GENERAL PROCESSOR (SGP)

    - GAAS D-MODE TECHNOLOGY

    - SGP FABRICATED AND TESTED IN FY87

    - OTHER DEVICES UNDER DEVELOPMENT BY DARPA AND ROCKWELL

  - DEMONSTRATE THE CHIP SET PERFORMING AN IMAGE COMPRESSION ALGORITHM (DPCM)

  - TO ASSURE VERSATILITY DESIGN AND ANALIZE A MIL-STD-1750 16-BIT COMPUTER BASED ON CHIP SET

C-3

GAAS PROCESSOR DEVELOPMENT

- APPROACH (CONT.)

    - CONTINUE IN FY87 STUDY TO DEFINE HIGH PERFORMANCE
      COMPUTER ARCHITECTURES (>1000 MIPS)

    - FOCUS ON E/D-MODE GAAS FOR HIGH PERFORMANCE SPACE
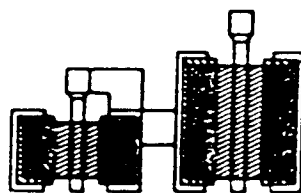   APPLICATIONS OF THE FUTURE

GSFC
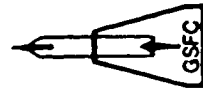
COMPARISON OF E/D DCFL WITH DEPLETION MODE BFL GATES
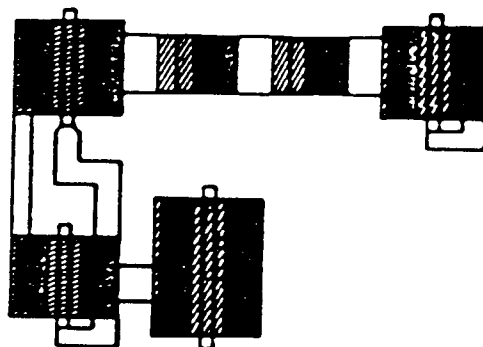
LAYOUT OF E-MODE AND D-MODE CIRCUITS

DEPLETION MODE (BFL)

V_T = -1.0V
V_{DD} = 2.5V
V_{SS} = -1.5V
AVE. POWER = 2.0 mW
INT. DELAY = 150 ps
POWER · SPEED = 300 fJ

ENHANCEMENT-MODE (DCFL)

V_T = 0.2V, -0.5V
V_{DD} = 2.0V
V_{SS} = —
AVE. POWER = 0.6 mW
INT. DELAY = 60 ps
POWER · SPEED = 36 fJ

Rockwell International

Microelectronics Research
and Development Center

2-192

NASA 8BS   DESIGN HIGHLIGHTS

o GALLIUM ARSENIDE TECHNOLOGY
   - BUFFERED FET LOGIC (BFL), ADAPTED FOR BUS ORIENTED ARCHITECTURE
   - DEPLETION - MODE MESFET ($-1.0v$ V_{TH})
   - 1.0 MICRON GATE LENGTH

o OPERATING SPEED: DC TO 200 MHz (GOAL)

o DIE POWER ESTIMATE
   - MAXIMUM 6.8w
   - AVERAGE 5.6w

o DIE SIZE: 193 MIL X 154 MIL

o NUMBER OF FETS: 7300

o CHIP I/O
   - 200 MHz DATA RATE
   - GaAs COMPATIBLE
   - 64 SIGNALS

NASA 8BS FUNCTIONAL BLOCK DIAGRAM
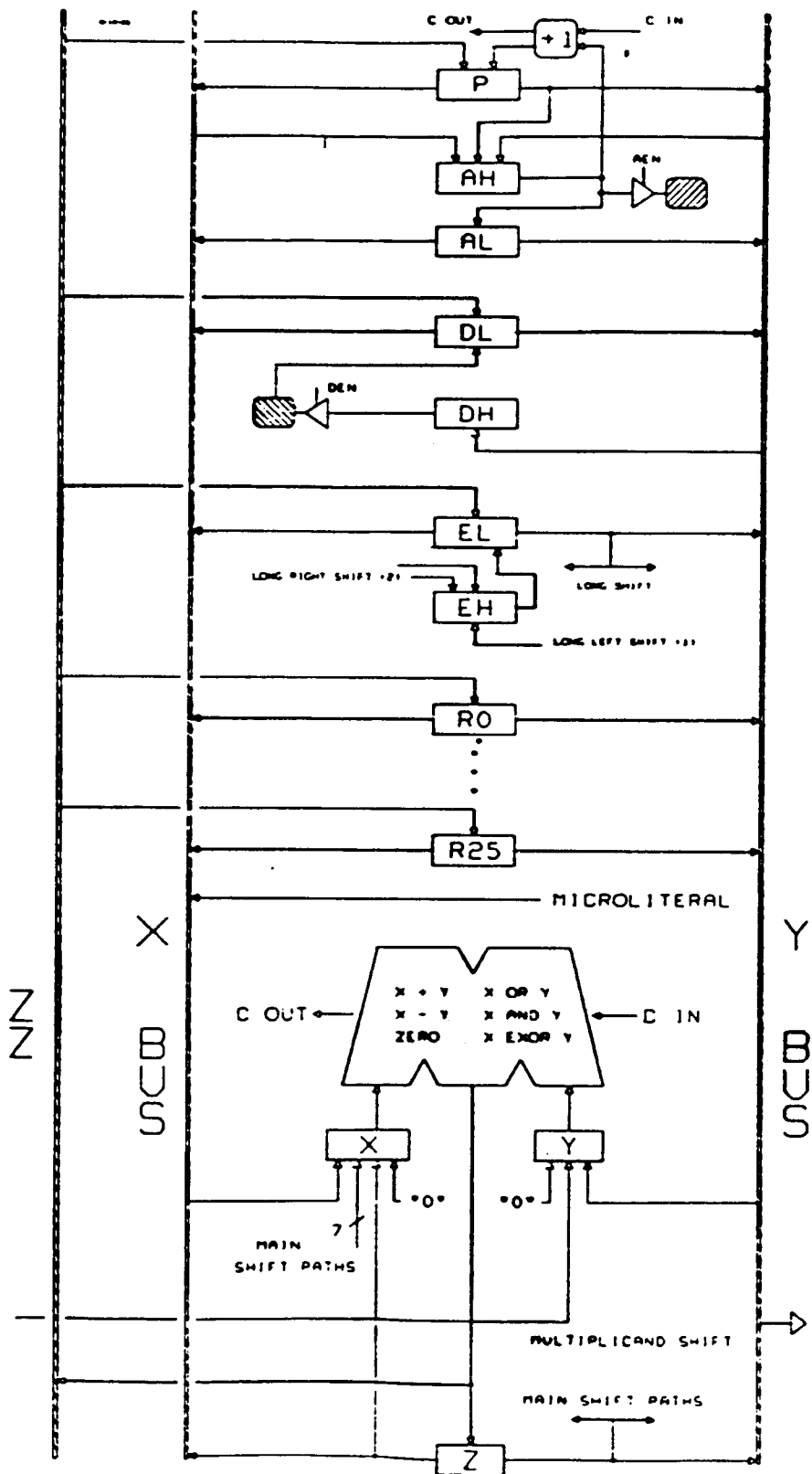
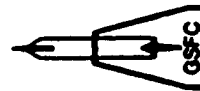# NASA 8BS   FUNCTIONS

o EIGHT-BIT ALU

    X + Y   X OR Y
    X - Y   X AND Y
    ZERO   X EXOR Y

o GENERAL EIGHT-BIT REGISTERS (R0-R25)

o 7 SPECIAL EIGHT-BIT REGISTERS
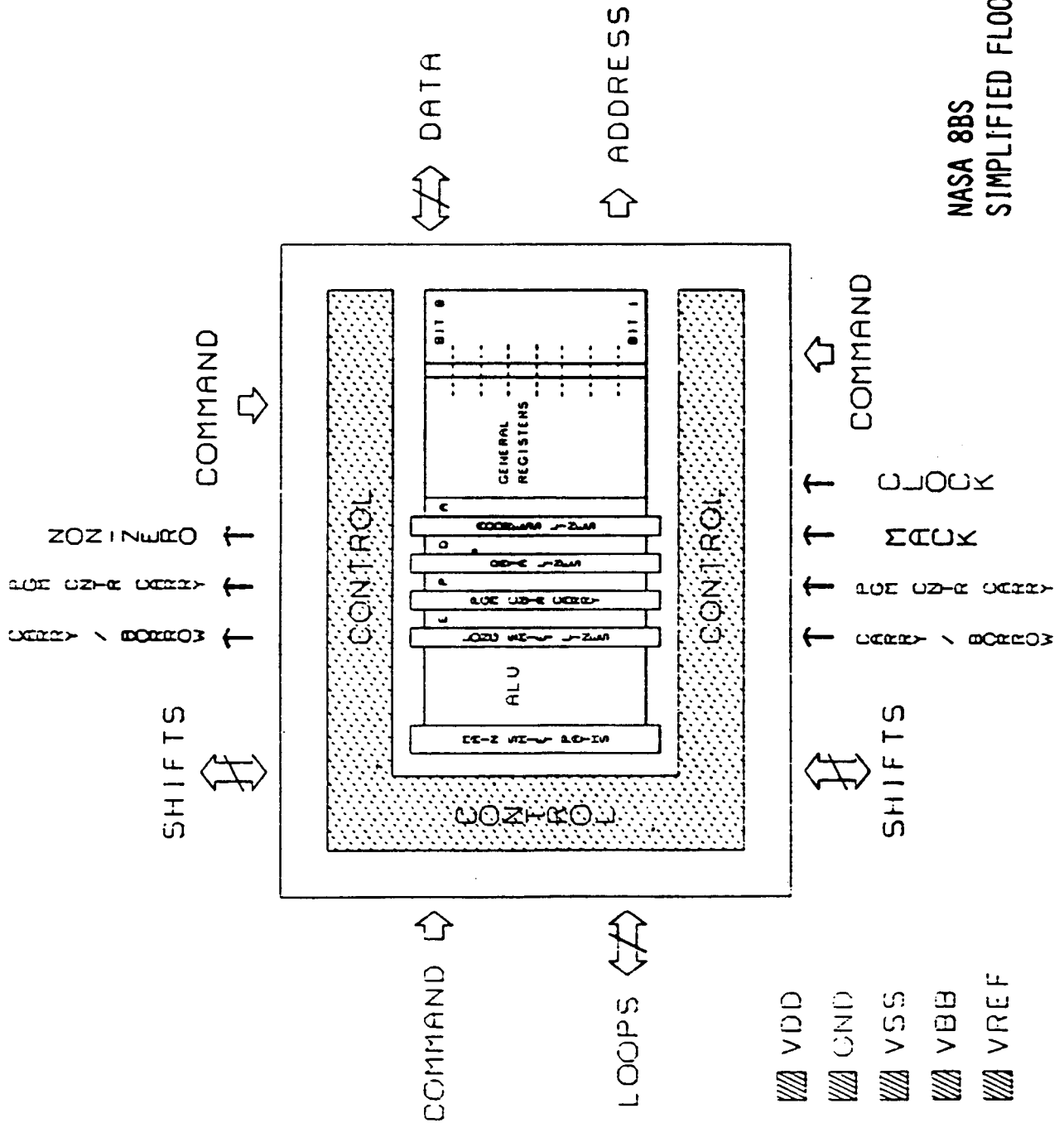
    - E   EXTENSION FOR MULTIPLY
    - D   DATA
    - A   ADDRESS
    - P   PROGRAM COUNTER
    - X   ARGUMENT TO ALU
    - Y   ARGUMENT TO ALU
    - Z   ALU RESULT

NASA BBS   FUNCTIONS (CONTINUED)

o THREE INTERNAL EIGHT-BIT BUSES
   - X-Bus
   - Y-Bus
   - ZZ

o SHIFTING
   Z --> X: L8, L4, L2, L1, R1, R2, R4, R8
   E --> E: L1, R1, R2
   Y-Bus --> Y: R1

o EIGHT-BIT PROGRAM COUNTER INCREMENTER

o LOOPS
   - CYCLE SHIFTS
   - OTHER NON-ADJACENT BS-TO-BS COMMUNICATIONS

o EIGHT-BIT ADDRESS BUS INTERFACE

o EIGHT-BIT DATA BUS INTERFACE

NASA 8BS
SIMPLIFIED FLOOR PLAN

DATA

ADDRESS

COMMAND

COMMAND

CLOCK

MPUX

NON ZERO

SUB INTR CARRY

ROT INTR CARRY

CARRY \ BORROW

CARRY \ BORROW

SHIFTS

SHIFTS

CONTROL

CONTROL

CONTROL

GENERAL
REGISTERS

BIT 0

BIT 1

ALU

COMMAND

LOOPS

VDD
GND
VSS
VBB
VREF

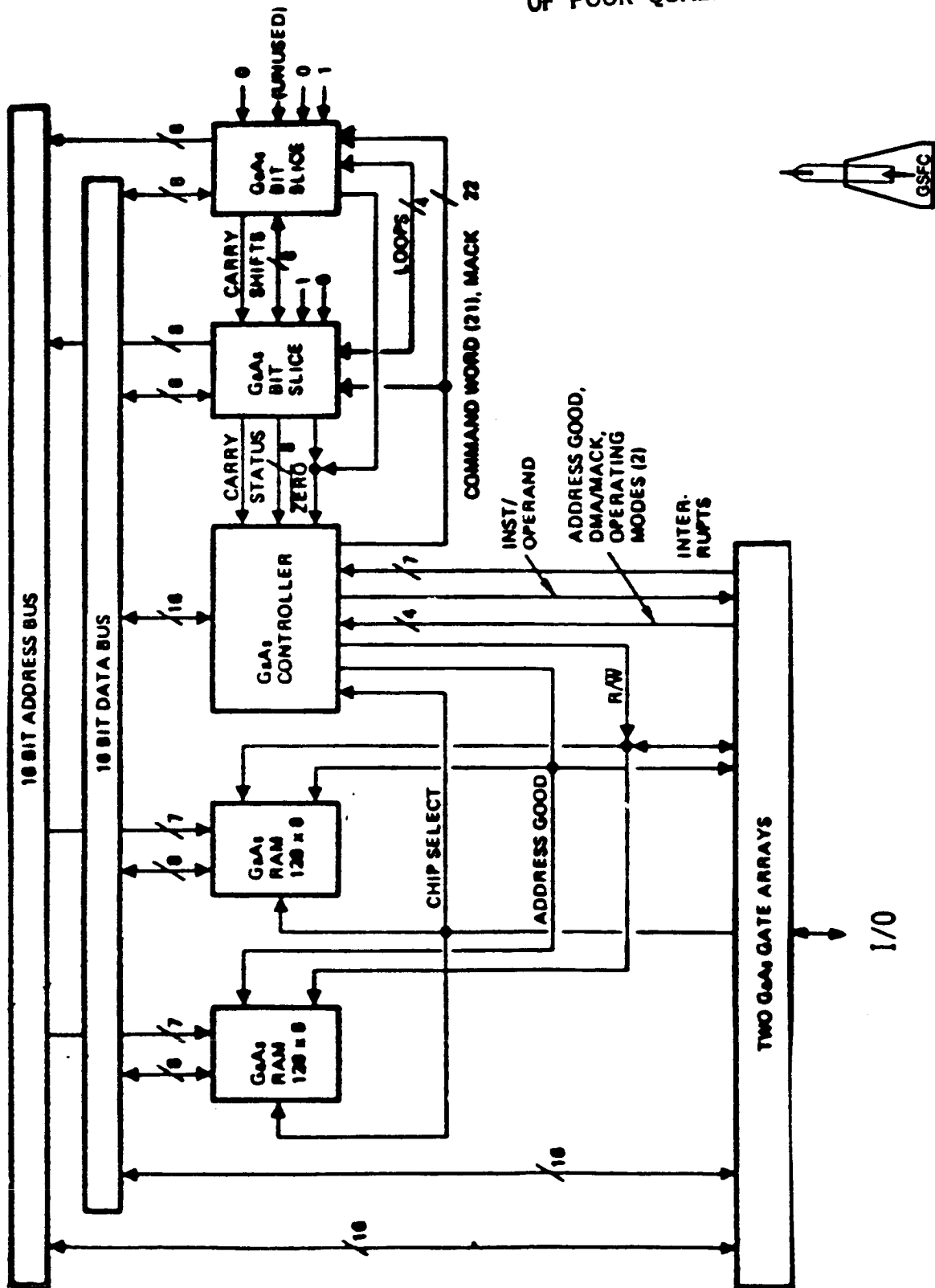GAAS PROCESSOR DEVELOPMENT

MIL-STD-1750 COMPUTER DESIGN HIGHLIGHTS

TECHNOLOGY   GAAS D MODE MESFET

WORD LENGHT   16 BITS

CLOCK RATE   200 MHz

MEMORY SPACE   64K WORDS

RADIATION HARDNESS:

    TOTAL DOSE $10^{**}8$ RADS(GAAS)

    SEU LATCH-UP   NONE

    SEU CHARACTERISTICS   TBD

POWER DISSIPATION   20 WATTS

SOFTWARE SUPPORT   AMPLE FROM DoD

GSFC

16 BIT ADDRESS BUS

16 BIT DATA BUS

(UNUSED)

0   0   1

GaAs
BIT
SLICE

CARRY   SHIFTS

1

LOOPS

COMMAND WORD (21), MACK   22

GaAs
BIT
SLICE

CARRY   STATUS

ZERO

GaAs
CONTROLLER

INST/
OPERAND

ADDRESS GOOD,
DMA/MACK,
OPERATING
MODES (2)

INTER-
RUPTS

R/W

GaAs
RAM
128 x 8

CHIP SELECT

ADDRESS GOOD

GaAs
RAM
128 x 8

TWO GaAs GATE ARRAYS

I/O

GSFC

1750A BLOCK DIAGRAM

KEY FUNCTIONAL ELEMENTS OF CONTROLLER

- INTERFACE WITH TEST EQUIPMENT - RESET, RUN, IDLE, SINGLE CYCLE, REGISTER CONTENTS READING OR LOADING

- MEMORY INTERFACE FOR FAST/SLOW RAM AND DMA

- BIDIRECTIONAL DATA PORT, INSTRUCTION REGISTER, MAP AND PIPELINE CONTROL

- MICROPROGRAM CONTROL ROM - STEP, BRANCH, 4 WORD STACK, 94 MAIN ROUTINES, 10 OPERAND FETCH ROUTINES FOR 187 INSTRUCTIONS

- ADDRESS REGISTERS AND COUNTERS
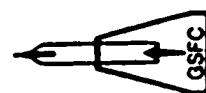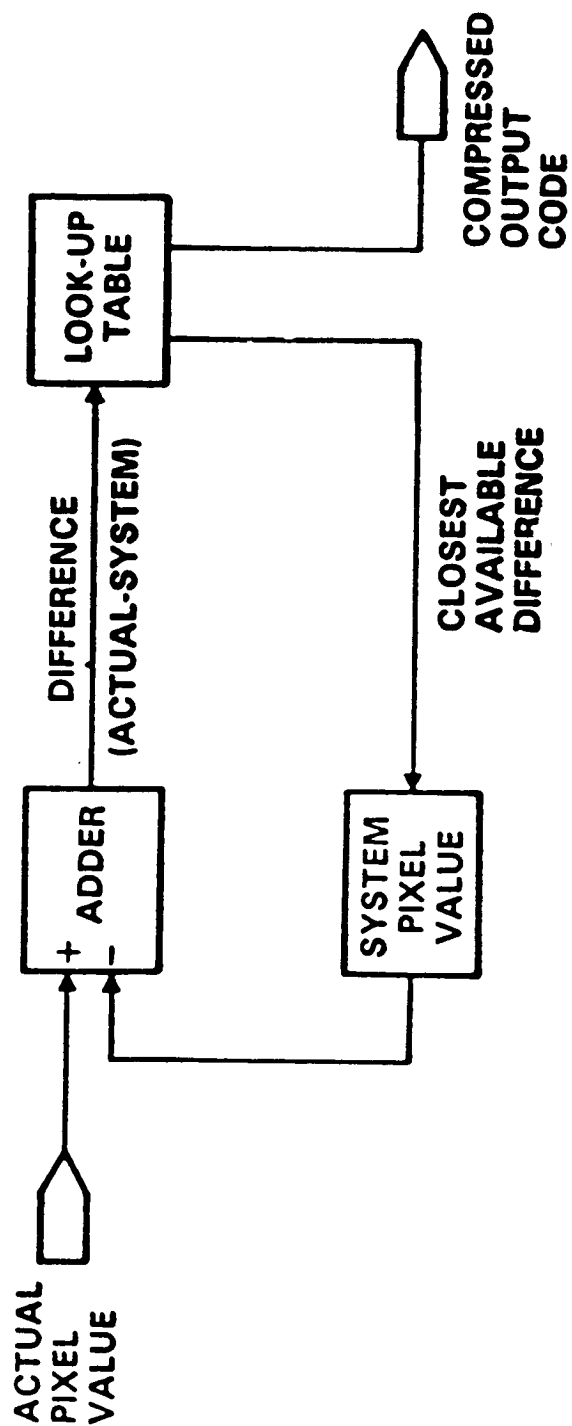
- STATUS LOGIC

- INTERRUPT LOGIC
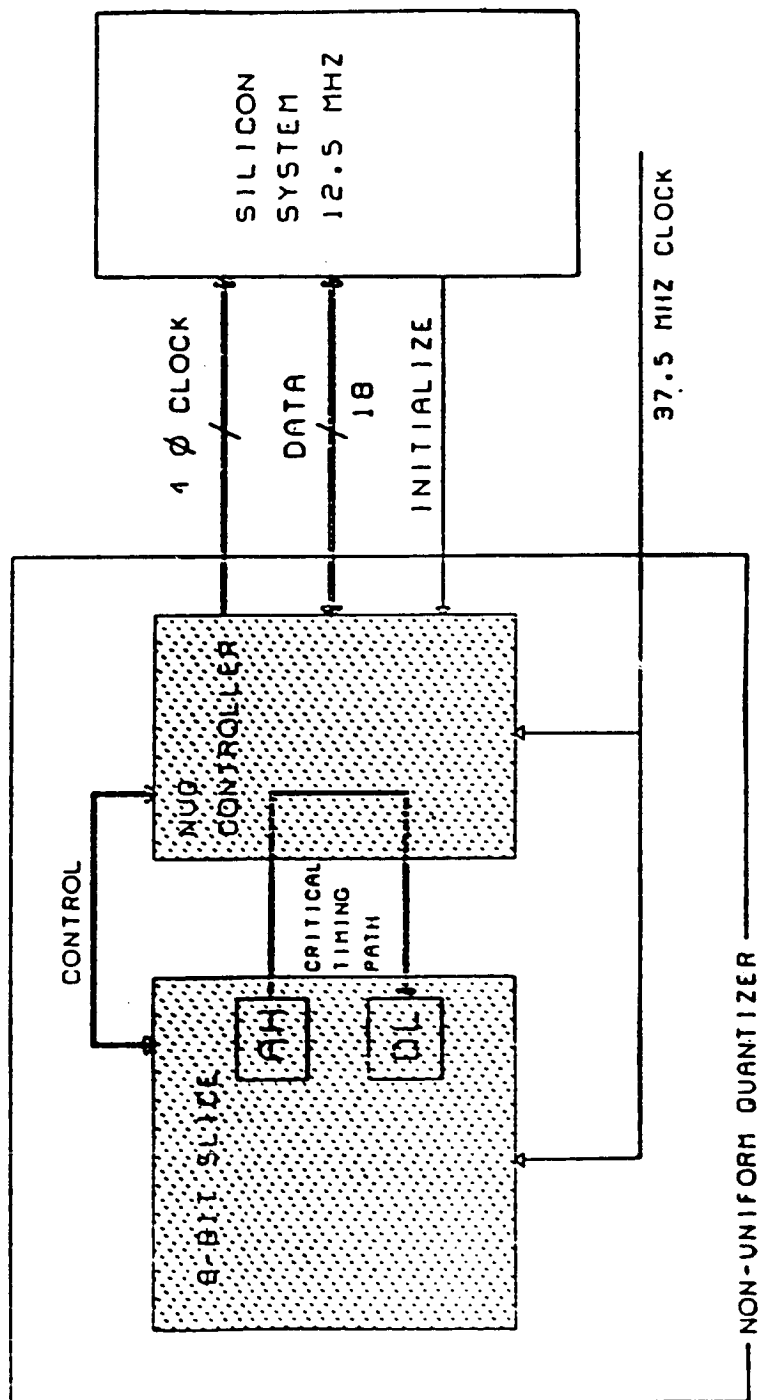
2-200
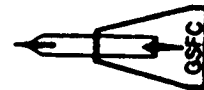
NASA NUO CONTROLLER   DESIGN HIGHLIGHTS

o STANDARD GaAs BUFFERED FET LOGIC

o OPERATING SPEED: DC TO 37.5 MHz

o DIE SIZE: 95 MIL (APPROX.) X 154 MIL

o CHIP I/O

- 37.5 MHz GaAs DATA RATE
- 12.5 MHz SILICON SYSTEM DATA RATE
- 44 SIGNALS

o BIAS SUPPLIES

- VDD (+2.5v)   POSITIVE LOGIC SUPPLY
- VSS (-2.0v)   NEGATIVE LOGIC SUPPLY
- GND (0.0v)   GROUND
- VCC (+5.0v)   POSITIVE CMOS/TTL DRIVER SUPPLY
- VBB (+2.5v)   POSITIVE GaAs DRIVER SUPPLY

NON-UNIFORM QUANTIZER SIMPLIFIED BLOCK DIAGRAM

ADC86-30013

ACTUAL PIXEL VALUE

ADDER

DIFFERENCE (ACTUAL-SYSTEM)

LOOK-UP TABLE

COMPRESSED OUTPUT CODE

CLOSEST AVAILABLE DIFFERENCE

SYSTEM PIXEL VALUE

GSFC

NASA NUQ   SYSTEM BLOCK DIAGRAM

GAAS PROCESSOR DEVELOPMENT

- FY88 ACCOMPLISHMENTS

- **COMPLETED CRITICAL DESIGN REVIEW OF 8-BIT SLICE GENERAL PROCESSOR (SGP) AND NON-UNIFORM QUANTIZER (NUQ) CONTROLLER:**

    - LOGIC DESIGN
    - CIRCUIT DESIGN
    - FLOOR PLAN
    - LAYOUT & XTRACE

- **COMPLETED DESIGN AND ANALYSIS OF MIL-STD-1750 CONTROLLER**

- **COMPLETED ANALYSIS OF DOD'S GAAS RISC PROCESSOR ARCHITECTURES**

GAAS PROCESSOR DEVELOPMENT

- **FY87** PROGRAM FOCUS

    - NON-UNIFORM QUANTIZER EFFORT:

        - MANUFACTURE WORKING TOOLS

        - FABRICATE TWO WAFER LOTS

        - DEVELOP TEST PLANS AND PROCEDURES

        - PURCHASE PROBE CARDS

        - WAFER PROBE 8-BIT SLICE GP AND NUQ CONTROLLER

        - DESIGN AND MANUFACTURE IC PACKAGE

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GAAS PROCESSOR DEVELOPMENT

- **FY87 PROGRAM FOCUS (CONT.)**

  - FOCUS EFFORT ON E/D MODE GAAS DEVELOPMENT:

    - DEVELOP PARALLEL/SERIAL & SERIAL/PARALLEL REGISTERS

    - EVALUATE 2900 GAAS FAMILY FROM VITESSE

  - CONTINUE TO IDENTIFY AND DEVELOP ONBOARD PROCESSING ALGORITHMS

GAAS PROCESSOR DEVELOPMENT

- FY88 PROGRAM FOCUS

  - DEVELOP ARCHITECTURES BASED ON THE 8-BIT SLICE GP AND A
    HARDWARE MULTIPLIER CHIP, CAPABLE OF PARALLEL AND PIPELINED
    DATA FLOW

- FY89 AND BEYOND PROGRAM FOCUS

  - DEMONSTRATE SELECTED ALGORITHMS AND ARCHITECTURES
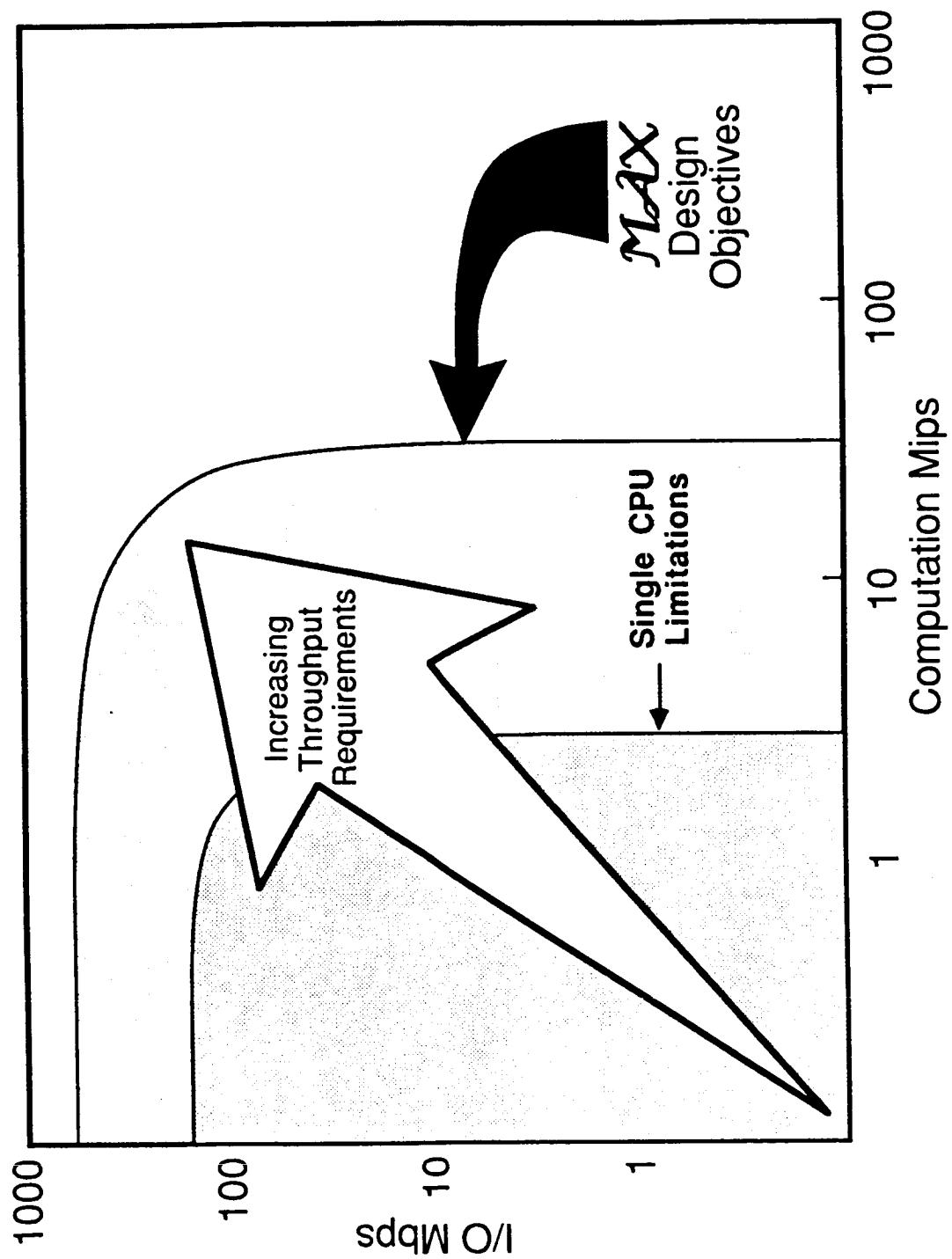
JPL

MAX

A High Speed, General Purpose
Multicomputer for Space Applications

November 20, 1986

Gary Bolotin

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Computational Requirements Summary

Increasing Throughput Requirements

MAX Design Objectives

Single CPU Limitations
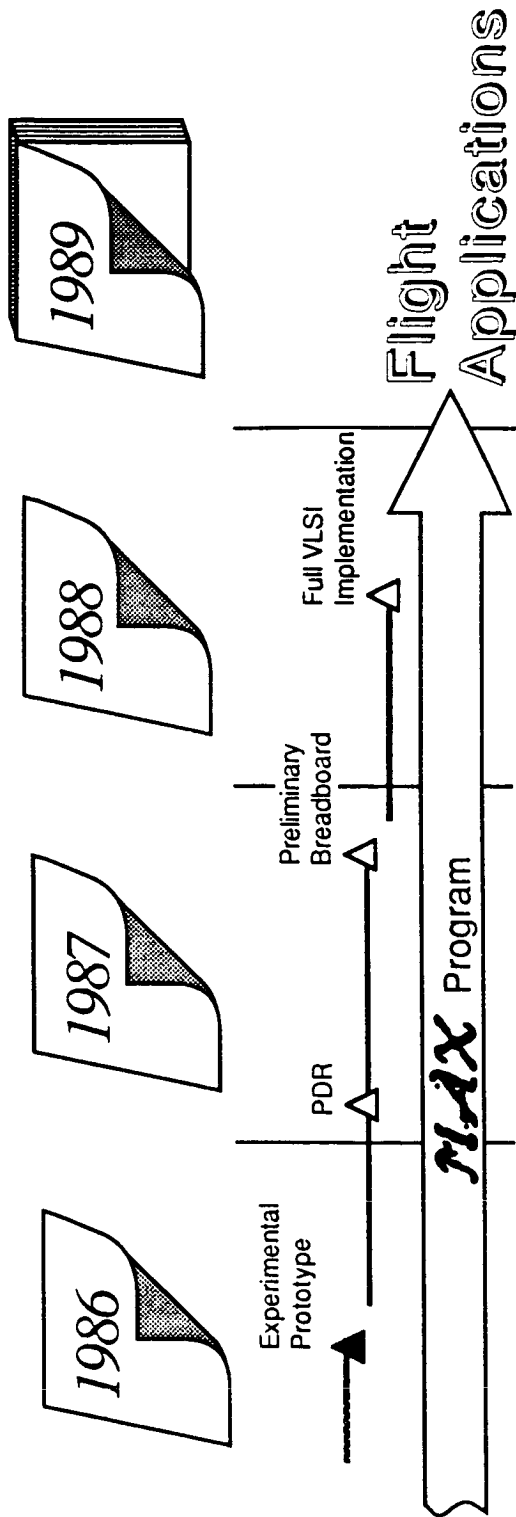
Computation Mips

I/O Mbps

JPL

Principle MAX Objectives

- New Device Technology

  - Faster, lower power, higher density
  - Radiation and Single Event Upset hard

- Powerful Software Methodology

  - High modularity
  - Sophisticated concurrency support
  - Configuration transparency

- Flexible Concurrent Architecture

  - Wide application range through modularity
  - Realizable in a variety of device technologies

- Fault Tolerance

  - Efficiently tailorable to application needs
  - Distributable for damage tolerance
  - On line repairability

JPL

MAX
Technology Roadmap

1986 1987 1988 1989

Experimental
Prototype

PDR

Preliminary
Breadboard

Full VLSI
Implementation

MAX Program

Flight
Applications

- Spacecraft
  Engineering Systems

- Robotics Applications

- High Data-rate Science
  Instruments

JPL

Device Technology

JPL

Device Technology

• Ultimate goal is a VHSIC realization

- Near term space qualifiability is an open issue

• Current implementation in Sandia National Laboratory components

- Previous flight qualification history.

- 2 micron, 10-15 MHz CMOS.

- Hard to >100 krad.

- SEU immune (>37 MeV / mg / cm^2).

- Emulation of NS32000 series components.
  - 32 bit μ-processor family.
  - Well suited to high level languages.

- Additional memory and glue components.

- Support for custom VLSI components.

JPL

Powerful Software Methodology

Two Models Compared

Control Flow

Control -
Sequential: flow spec.
by instructions (ip)

Data passing -
By reference: indirectly
through shared memory
(variables)

Concurrency -
Explicit: branching
control flow (fork)

Synchronization -
Explicit: convergent
control flow (join)

**Separate mechanism
for each**

Data flow

Control -
Parallel: flows with
data (tokens)

Data passing -
By value: directly between
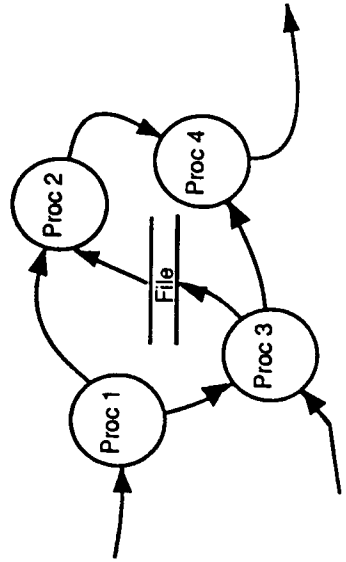instructions (tokens)
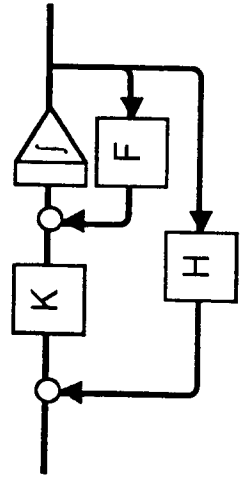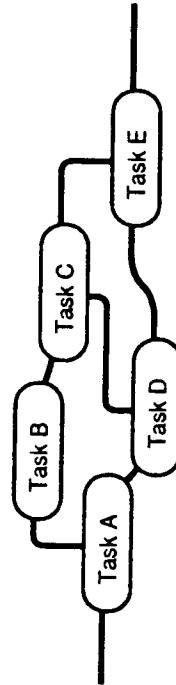
Concurrency -
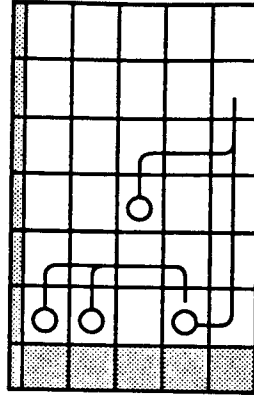Implicit: token
proliferation

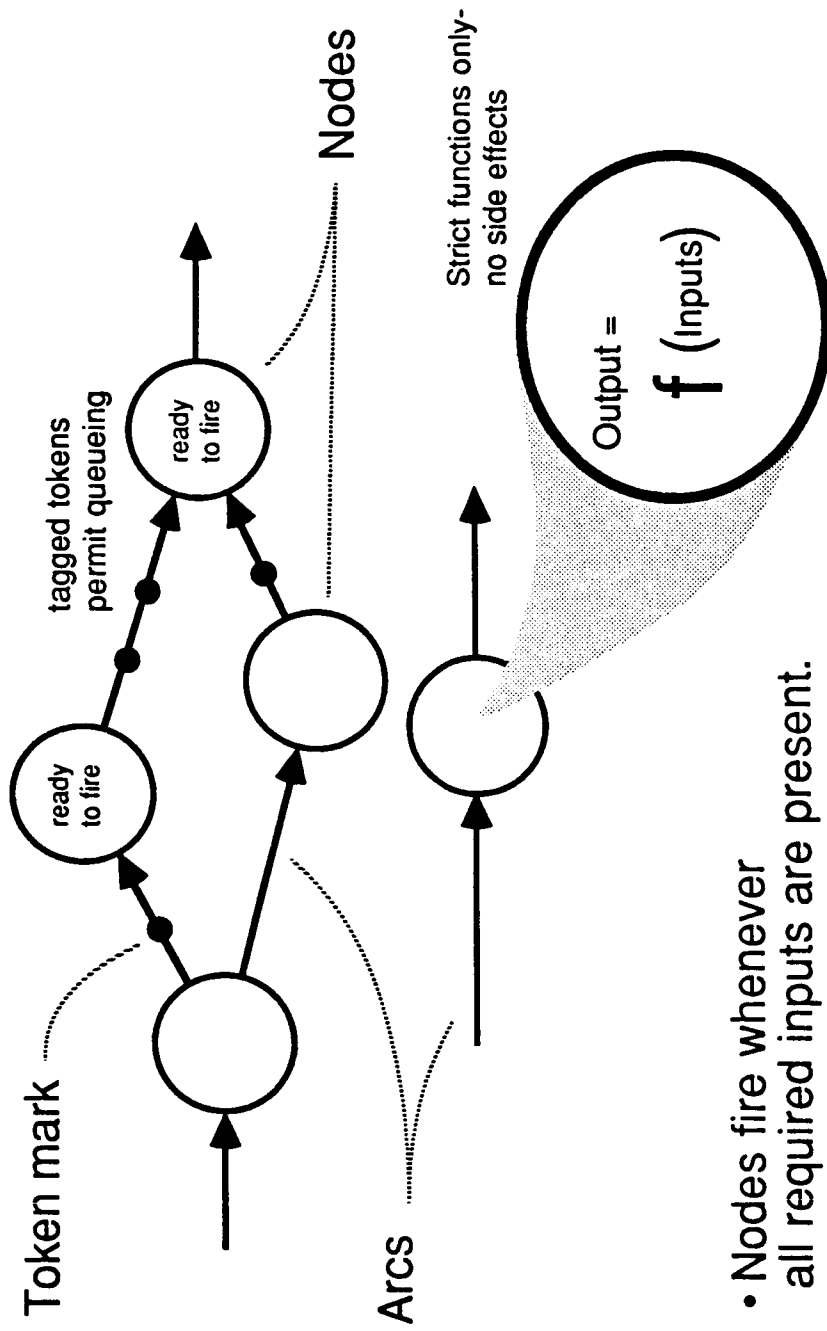Synchronization -
Implicit: token
matching

**Single unifying
mechanism**

The Data Flow Concept

- System functions activated by the flow of information

- Relationships often represented by Data Flow Graphs

- Familiar models...

  - Spreadsheet programs
  - PERT charts
  - Signal flow diagrams
  - DeMarco structured analysis diagrams

Data Flow Formalities

Nodes

tagged tokens
permit queueing

ready
to fire

ready
to fire

Token mark

Arcs

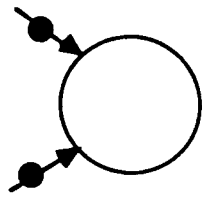Strict functions only-
no side effects

Output =
$$\mathbf{f} \, (\text{Inputs})$$

- Nodes fire whenever
  all required inputs are present.

- Tokens can be created or destroyed,
  but never changed

- Strict functions only, no side effects

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Data Flow

Graph Types:

Simple:

Recursive:

JPL

Firing (Scheduling) Rules:

Simple Inputs:
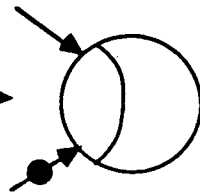
Merge Inputs:
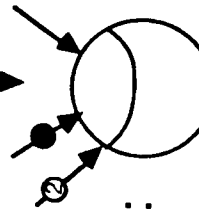
Select Inputs:
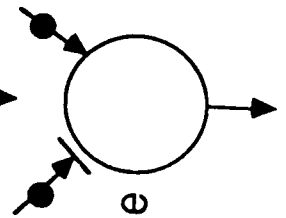
Nonconsumable Inputs:
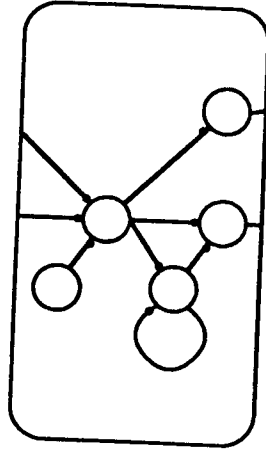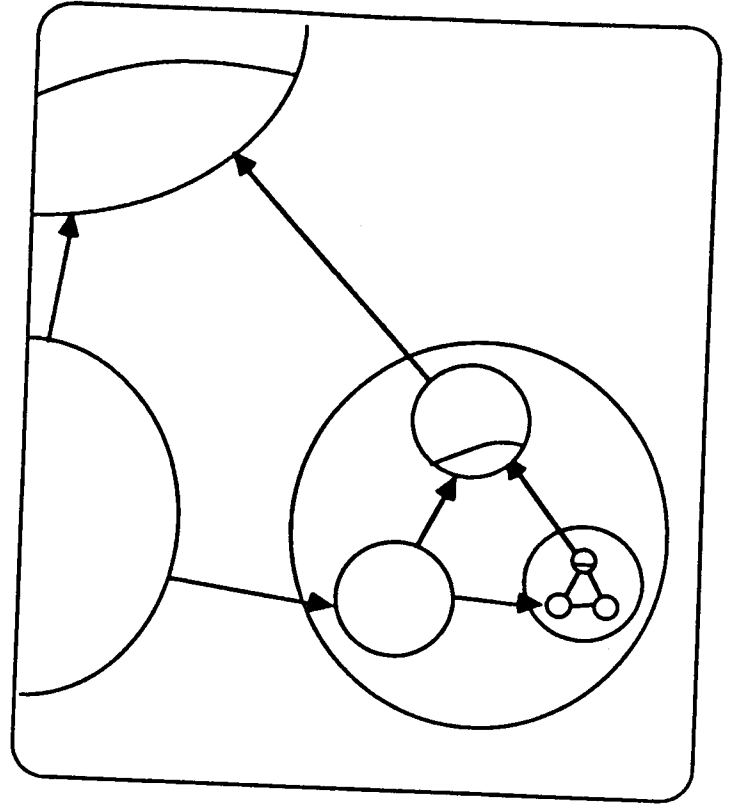
High vs. Low Resolution Data Flow

JPL

- High resolution
  - Simple data (numbers, booleans, etc)
  - Simple operations (arithmetic, logic, etc)

- Low resolution
  - Complex data (arrays, structures, lists, etc)
  - Complex operations (matrix ops., search, sort, etc)

Efficiency

Low   Resolution   High
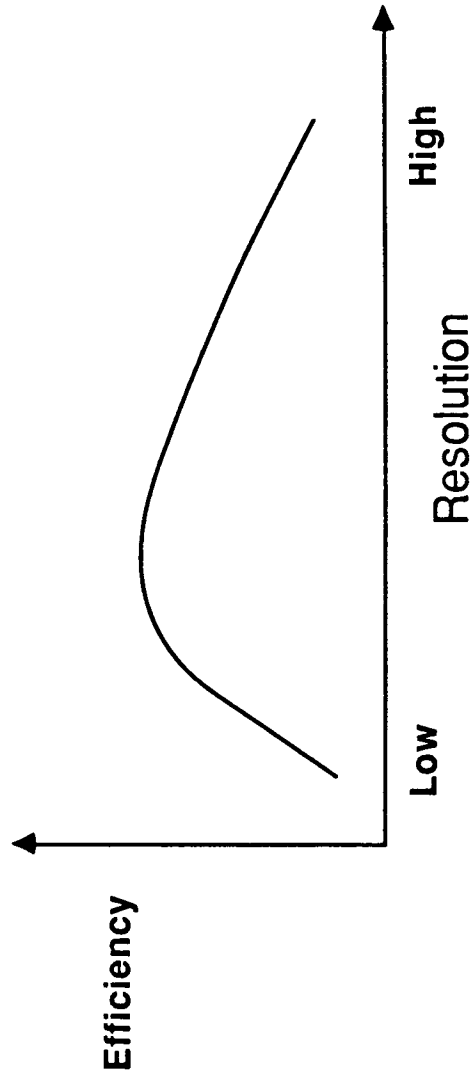
Data Flow Software Design

JPL

STRUCTURE scanner_packet =
BEGIN
   2.5, 30, 12, 34, 45, 58, 33, 0,
    1.8, 44, 13, 40, 40, 49, 30, 0,
    1.9, 31, 12, 39, 41, 55, 28, 1,
    1.8, 31, 13, 34, 44, 54, 28, 0
    ...
END

Filter (scanner_packet , running_average)
SCAN_RECORD scanner_packet;
INTEGER running_average;
BEGIN
   /* high level language statements */
   ...
   output (smoothed_scanner_packet);
   output (new_running_average);
   ...
END

Decom.

Filter

Comp-ression

Telem. Format
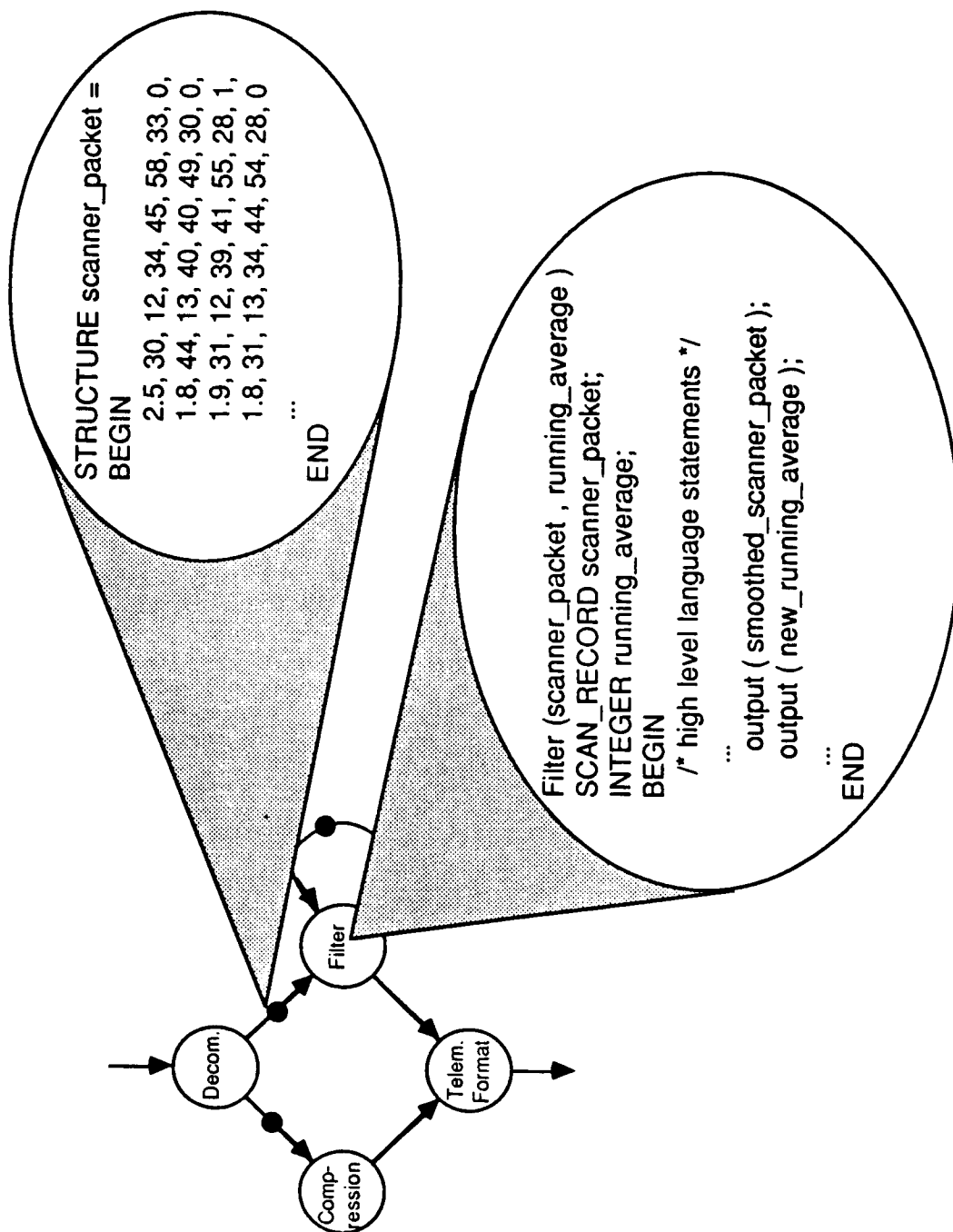
JPL Low Resolution Data Flow Advantages

• Concurrency specification facilitated

• Highly modular code
  - Details of code hidden at system level
  - Design specification, coding, test, and maintenance
    in small, decoupled pieces

• System state completely embodied in tokens
  - No other context to preserve through faults or interruptions
  - Need compare or checkpoint only tokens

• Unified approach to data & control lowers overhead
  - Token data
  - Meshwork packets } *common structure*
  - Memory blocks
  - Code segments

HYPHOS

The MAX Operating System

JPL

- Fully distributed

  - One copy on each module
  - Cooperation via global bus

- Layered design

  - Conventional multi-tasking and I/O at lower level
  - Data flow programming model at high level

- Tailored for real time applications

  - Time / event operations
  - Prioritization of responses

- Transparently implements fault tolerance

JPL

Flexible Concurrent Architecture

Topology examples

JPL
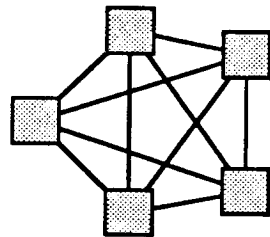
- **Fully connected**
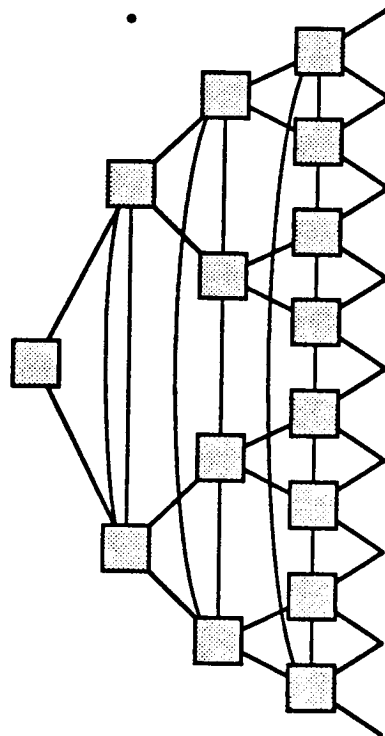
- **Augmented Trees/rings**

- **Hypercube**

JPL

More topology examples
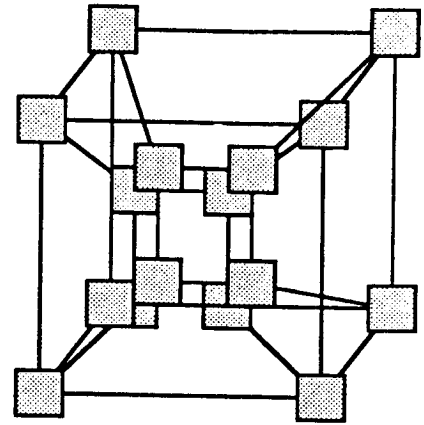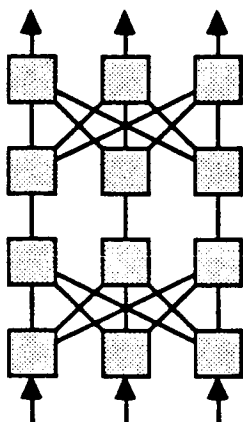
- **Multi-staged pipeline**
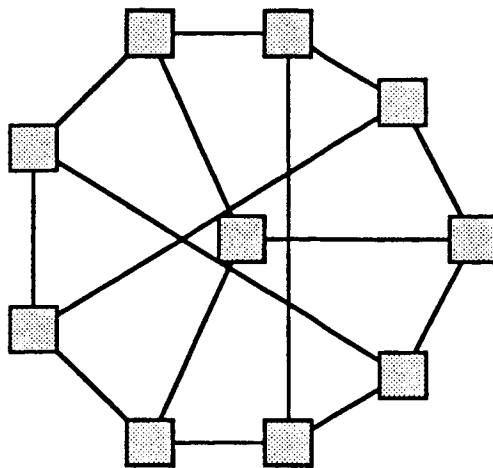
- **(d,k) complete**
  d = 2, k = 3
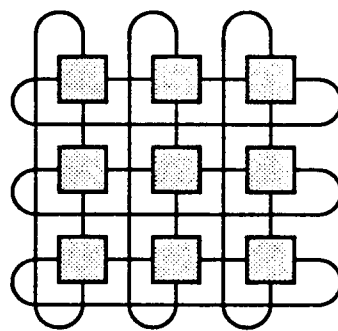
- **Torroidal mesh**

MAX Hardware Architecture

JPL
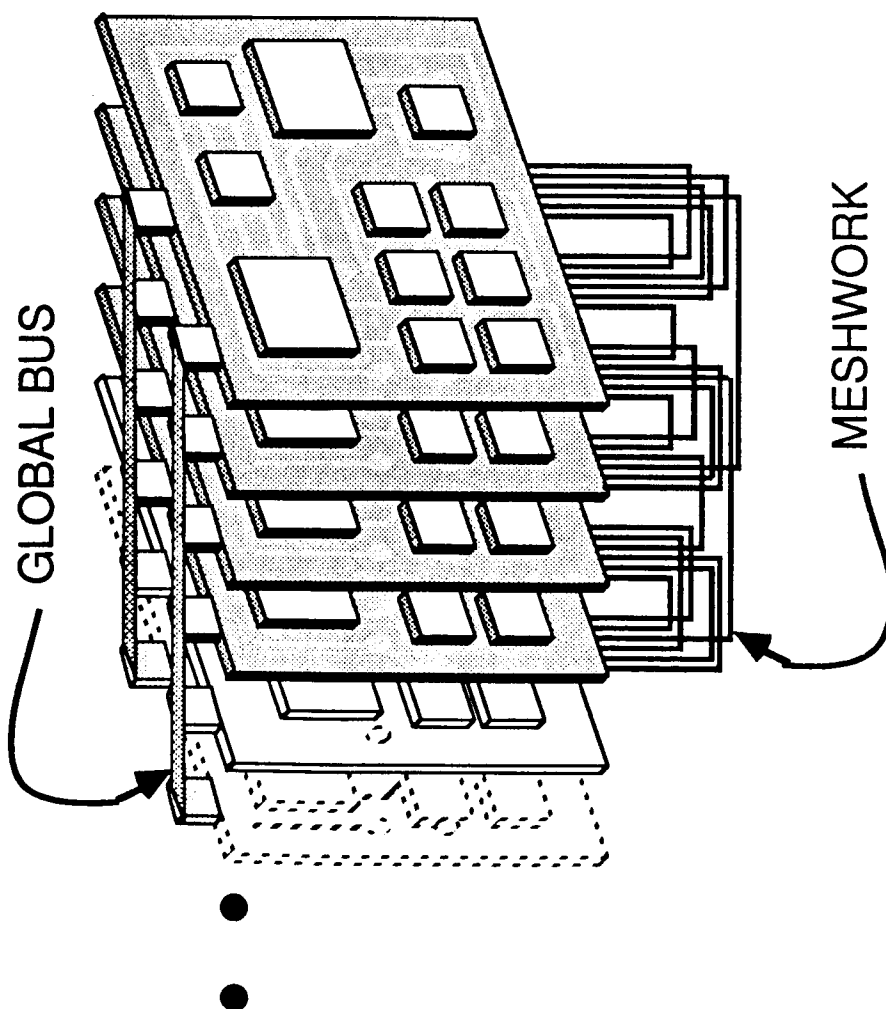
- FULLY DECENTRALIZED

- ANY NUMBER OF IDENTICAL PROCESSING MODULES

- NO SHARED MEMORY BETWEEN MODULES

GLOBAL BUS

MESHWORK

MAX Module Configuration

JPL

- DUAL PROCESSOR DESIGN
- SEPARATE LOCAL BUS & MEMORY FOR EACH CPU
- COMMUNICATION THROUGH SHARED MEMORY
- DMA I/O SUPPORT
- FPU CO-PROCESSOR
- OFF BOARD BUS
- SINGLE BOARD DESIGN
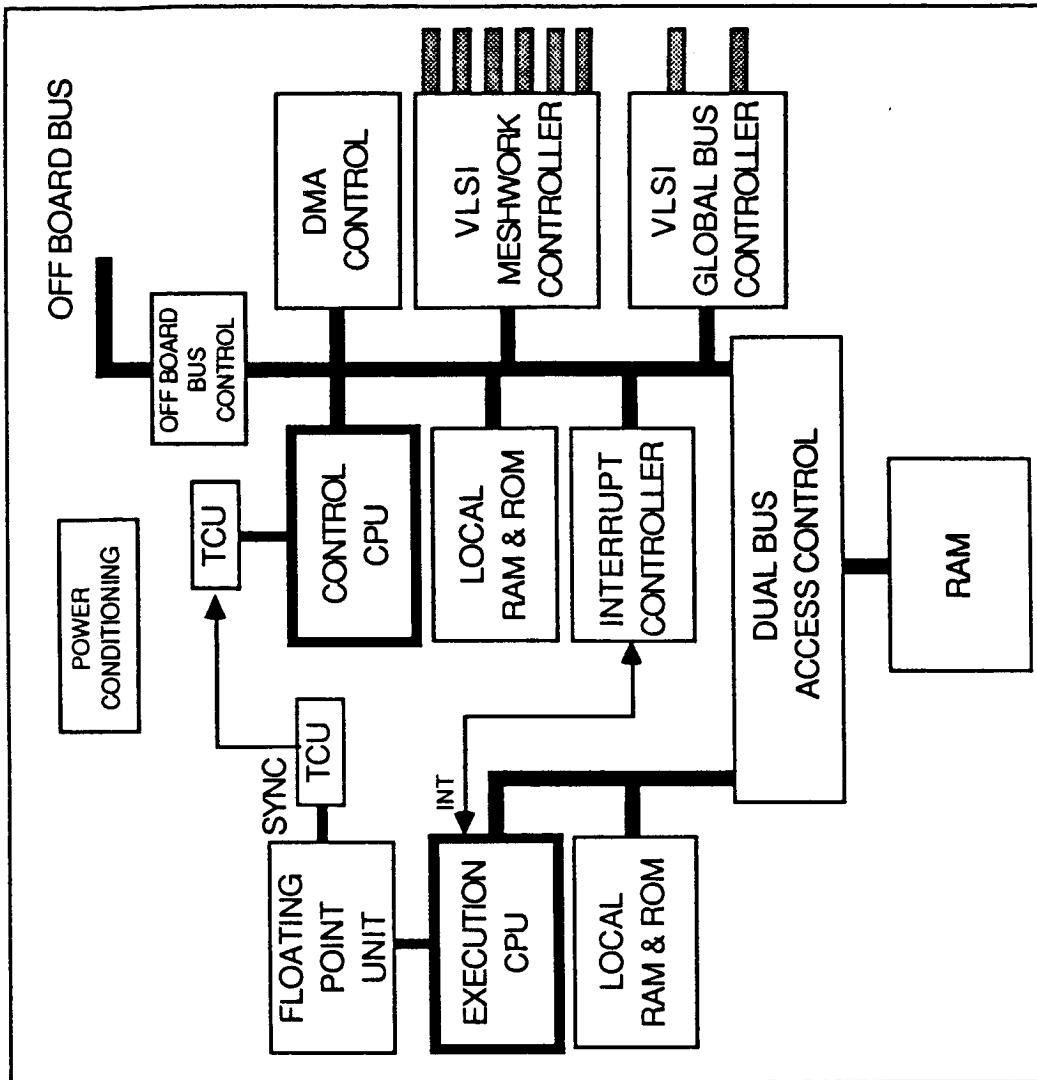
VLSI Meshwork Controller Features

JPL

- On-chip circuit switching
- Implements HDLC communication
  with on-chip CRC generation and error detection
- Up to 10Mhz operation
- Optional Manchester II coded data transfer
- DMA or interrupt driven

Output to other modules

32 bit data/ address bus

Crossbar Switch

Trans- mitter

Receiver

Input from other modules

VLSI Global Bus Controller
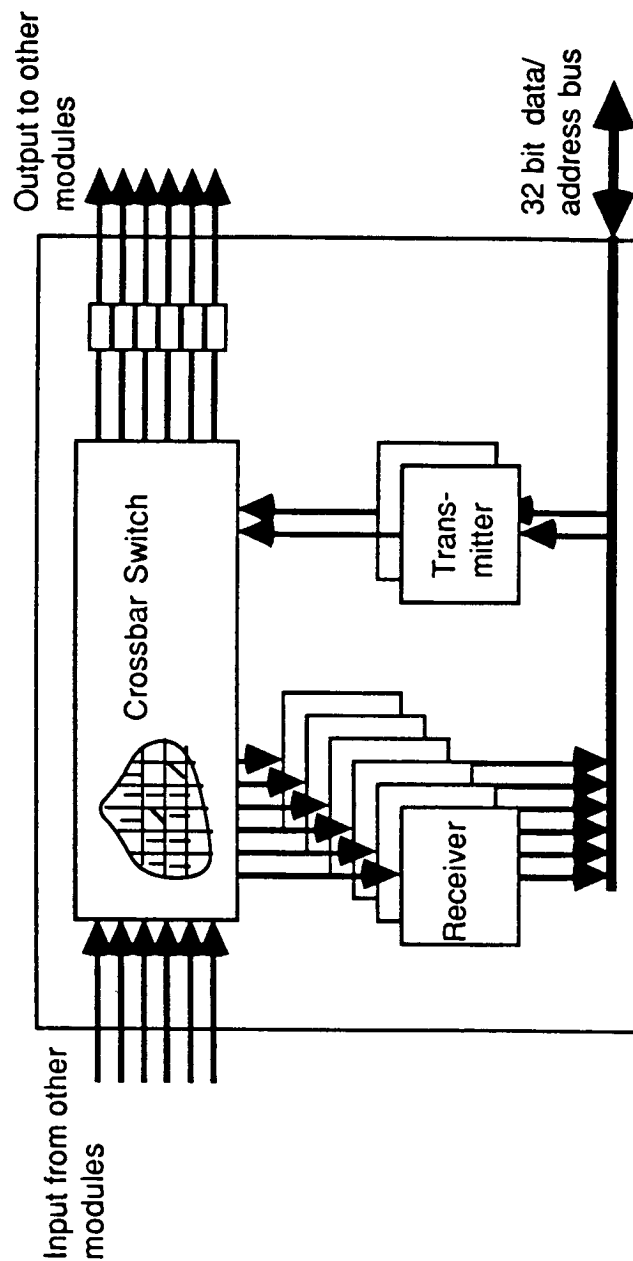
Features:

- 0.5 to 10 Mhz programmable baud rate
- Broadcast mode
- Fully distributed operation
- Deterministic (worst case) access delay
- Round robin access during heavy loading
- Multiple access during light loading
- Minimal data traffic, only control information
- Global system time synchronization

Transmitter

Receiver

Watch dog timer

System Time

Interface to 32 or 16 bit internal module bus

Fault Tolerance

JPL

JPL
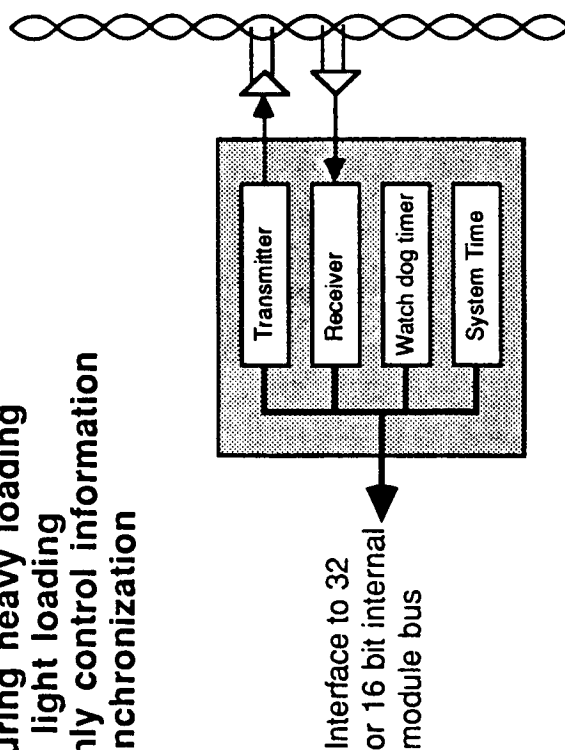
Fault Tolerance

- Software

  - Transparent redundancy
  - Distributed operating system
  - Multiple copies of application software
  - Triplicate and vote option for data-flow graph functions

- Hardware

  - Meshwork can route around failed boards
  - Dual global bus design

JPL

MAX
Technology Roadmap

1986   1987   1988   1989

Experimental Prototype

PDR

Preliminary Breadboard

Full VLSI Implementation

MAX Program

Tools & Techniques

Custom Components

Radiation Hardened Devices

Pathfinder (SDIO)

Mariner Mark II (NASA)

JPL VLSI Technology Programs

Sandia CMOS III Components (DoE/DoD)

Flight Applications

- Spacecraft Engineering Systems

- Robotics Applications

- High Data-rate Science Instruments

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JPL

Extensions of Current Work

- Alternate load balancing heuristics
  - Application specific
  - Degraded systems
- Data flow algorithms
  - Concurrency techniques
  - Re-usable code
- Advanced development software
  - Graphical compilers
  - Dataflow languages
  - Embedded system simulation tools

Massively Parallel Processor (MPP)

The MPP is:

- 16,384 PROCESSORS (on a 128 by 128 grid)

- HERE AND WORKING

- BEING EXPLOITED FOR SCIENTIFIC RESEARCH IN:

  Physics

  Earth Science

  Image & Signal Processing

  Computer Science

- CONVENIENTLY PROGRAMMABLE

OVERVIEW

MPP Status

1977 — CONCEPT

1983 — DELIVERED TO GODDARD

1983 to present — SYSTEM AND APPLICATIONS SOFTWARE DEVELOPMENT

1985 — BROAD USER COMMUNITY

THE MPP IS NOW BEING DEVELOPED AS A NATIONAL RESOURCE FOR PARALLEL ALGORITHM RESEARCH

GSFC
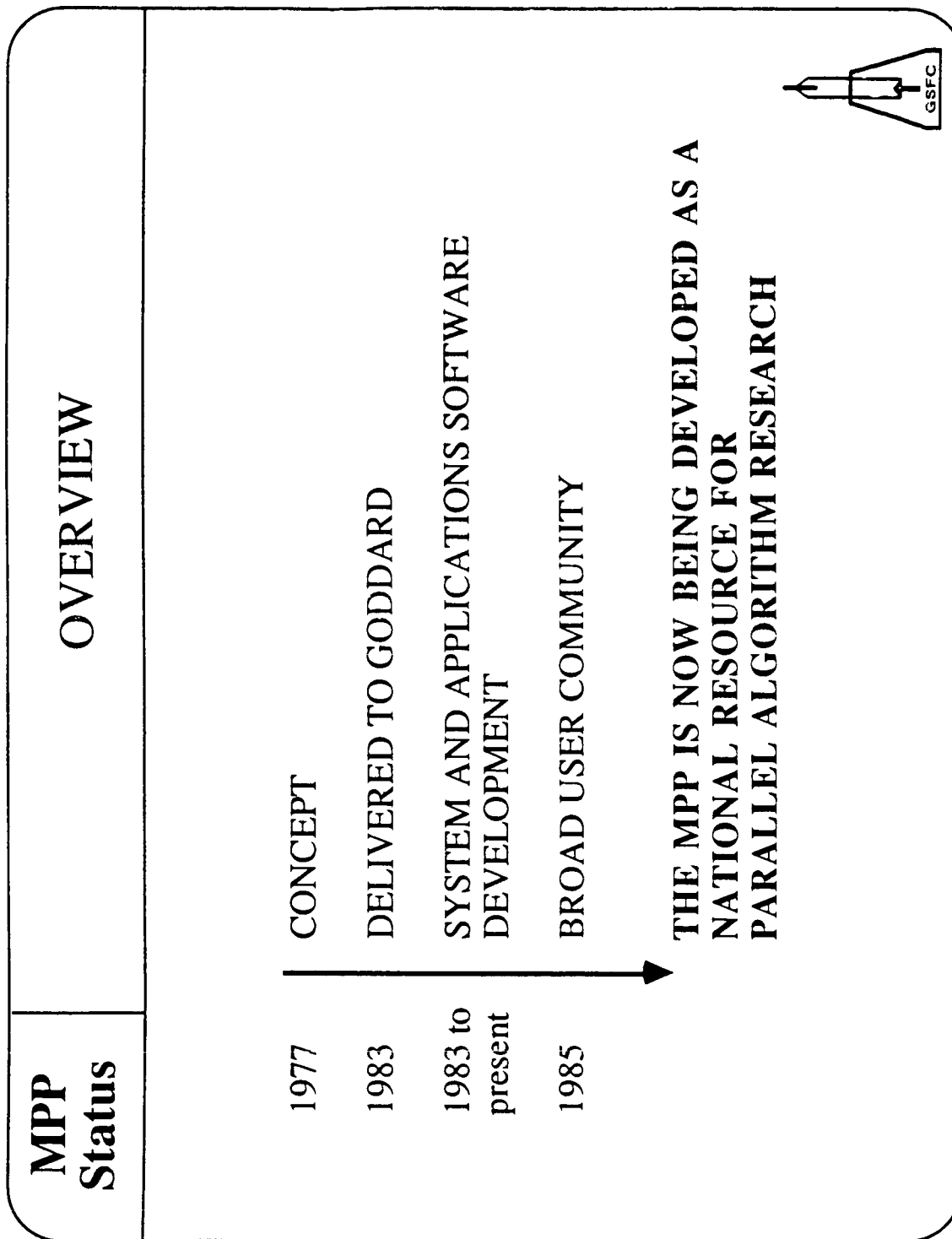
MPP Status	WORKING GROUP
	Space Science and Applications Notice (AN)
	'Computational Investigations Utilizing The Massively Parallel Processor'
	PROPOSALS ACCEPTED TO DATE
	9 in Image / Signal Processing
	5 in Earth Science
	10 in Physics (Plasma, Astro, Atomic)
	11 in Computer Science
	4 in Graphics

MPP USER SITES

■ RESEARCH LABS

1 SPACE TELESCOPE SCIENCE INSTITUTE
2 NBS
3 SOUTHWEST RES. INST.
4 KMS FUSION
5 GSFC
6 LANGLEY RESEARCH CENTER
7 JPL
8 NRL
9 USDA
10 TRW
11 NSA

● UNIVERSITIES

1 STANFORD
2 CASE WESTERN
3 UN. OF MARYLAND
4 STATE UN. OF NY
5 COURANT INSTITUTE
6 UN. OF IOWA
7 FLORIDA STATE
8 UN. OF CALIFORNIA
9 UN. OF S. CALIFORNIA
10 NC STATE UN.
11 UN OF AKRON
12 INDIANA UN.
13 UN. OF ALABAMA
14 HOFSTRA UN.

NASA/GSFC

85A1879-14

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MPP USER APPLICATIONS

MPP Status

MODELING

Galaxy Evolution
Laser Simulation
Ising Spin Simulation (Atomic Physics)
Plasma Simulation
Navier Stokes Code

IMAGE & SIGNAL PROCESSING

Detection & Classification Of Galaxies
Analysis Of Biomedical Images
Reconstruction Of Coded Aperture X-ray Images
Contextual Classification
Registration Of Very Large Images
Generation Of Topographic Maps From Imagery
Detection Of Geological Fracture Patterns
Synthetic Aperture Radar

GRAPHICS

Space Plasma Graphics Animation
Ray Tracing

COMPUTER SCIENCE

Graph Theoretic Problems
Cellular Automata
Linear Systems Solutions
Forth
Applicative Programming Storage Architecture

ASTRONOMICAL IMAGE RESTORATION
Dr Sara Heap, GSFC, Code 681

MPP Applications

METHOD: Algebraic solution of a large linear system (10^5 by 10^5 elements)

FEATURES:
- Uses block Jacobi method with iteration
- Constrained solution
- Allows variation of point spread function across image

APPLICATIONS:
- Develop finer detail in imagery
- Eliminate scattered light from nearby bright object
- Enhance sensitivity

STATUS: Operational for 512 by 512 images

MPP Applications	GRAPHICS MODELS OF SPACE & EARTH SCIENCE DATA Lloyd Treinish, GSFC, Code 634

METHOD: MPP used to partially render a uniform three dimensional surface from a non-uniform data set. A Megatek Merlin graphics terminal performs the final rendering and display.

FEATURES:

- User does not know or care that the MPP is being used

- Transparently accessible from remote DECnet nodes

- Animated sequences of frames are stored in the Merlin and displayed

- Input data is in the Common Data Format (CDF) developed by the National Space Science Data Center, GSFC

APPLICATIONS:

- Rapidly produce visual representations of large, complex, multidimensional space science data sets

STATUS: operational

CONTEXTUAL CLASSIFICATION
Dr James Tilton, GSFC, Code 636

MPP
Applications

METHOD:

Baysian multispectral classifier, expanded to use more than one pixel of information

FEATURES:

• Class of each pixel in image determined by statistics based on itself & other pixels (ie. 4 nearest neighbors typically)

• Computationally intensive - order of $m**p$ calculations per pixel, where: m is the number of classes
and: p is the number of pixels in the context

APPLICATIONS:

• Landsat image classification

• Classification of higher resolution earth observation imagery (such as SPOT)

STATUS:

• Operational under batch for image size up to 8192 by 8192

• 512 by 512 image with 5 classes takes ~30 minutes wall clock

MPP Applications	AUTOMATIC GENERATION OF TOPOGRAPHIC MAPS
	Dr James Strong, GSFC, Code 636

METHOD: Hierarchical warp stereo technique matches corresponding areas in two images

FEATURES:
- Automatic
- Iterative - initial step done at low resolution, each succeeding steps done at higher resolution
- Supports interactive experimentation with alternative parameters

APPLICATIONS:
- Topographic map generation
- object tracking

STATUS: operational

NEURAL NET MODELING
Dr Harold Hastings, Hofstra University

MPP Applications

METHOD: Learning experiments performed on a large network of McCulloch-Pitts neurons (threshold devices) connected by synapses with stochastic conduction thresholds.

FEATURES:

- Uses a stochastic model for learning which assumes that noise is beneficial to learning

- An anealing system - combines random search with gradient search

- Applies equally well to the work of Hopfield, Hinton et al, and Geman and Geman

APPLICATIONS:

- Control systems

STATUS: Artificially dumb system operational

COMPUTING FRACTAL PATCHES
Dr Michael McAnulty, University of Alabama

METHOD: Recursively sub-divide a patch. Map the recursion spatially onto the array. The value of each new patch is based on the parent patch plus a stochastic contribution.

FEATURES:
- Simple to describe
- Clouds look like clouds

APPLICATIONS:
- Automatic generation of texture

STATUS: Operational

COMET HALLEY LARGE-SCALE IMAGE ANALYSIS
Dr Dan Klinglesmith, GSFC, Code 684

MPP
Applications

OBJECTIVE: For digital images up to 6000 by 6000, implement image analysis tools: image rotation, rubber sheet stretching, registration and resampling, noise removal, and photometric calibration

FEATURES: Image rotation and rubber sheet stretching implemented with an algorithm that preserves photon count.

APPLICATIONS: Remapping of photographs of Halley's Comet taken by many telescopes onto one common frame of reference

STATUS: Image rotation and rubber sheet stretching operational for images up to 6000 by 6000

FEEDBACK FROM THE MPP USERS

Sept 26, 1986

STATEMENTS:

- The process of rethinking algorithms to make them parallel was extremely useful

- Many effective parallel algorithms exist that are not well known outside computer science

- Many projects are using simplified models due to MPP data memory constraint - they want 10 to 100 times more memory

- If Parallel Pascal showed up on another machine, their code would probably port

- "the MPP was easy to use"

REQUESTS:

- Higher network data rates to remote user sites

- Less oversubscribed MPP host computer

- Improved portable software development environments

- More development by NASA of general library routines

- Real-time video output from the array

CONCURRENT PROCESSING RESEARCH

CODE R

506-44-11   J. DORBAND

OBJECTIVE

Develop Algorithms Not Typically Viewed as Effectively Processed by Highly Parallel Computer Architectures

APPROACH

- General Ray Tracing

- Solution of Sparse Linear Systems

- Parallel LISP

- Language Compiling

- Recursive Function Evaluation

OAST

COMPUTER SCIENCE/DATA SYSTEMS
TECHNICAL SYMPOSIUM

ADVANCED DIGITAL SAR PROCESSOR
(ADSP)

Tom Bicknell

JPL

November 20, 1986

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

SAR DATA ACQUISITION AND PROCESSING

TARGET SIGNAL

SIGNAL RECORDING

IMAGE DISPLAY

IMAGE RECORDING

SAR PROCESSOR
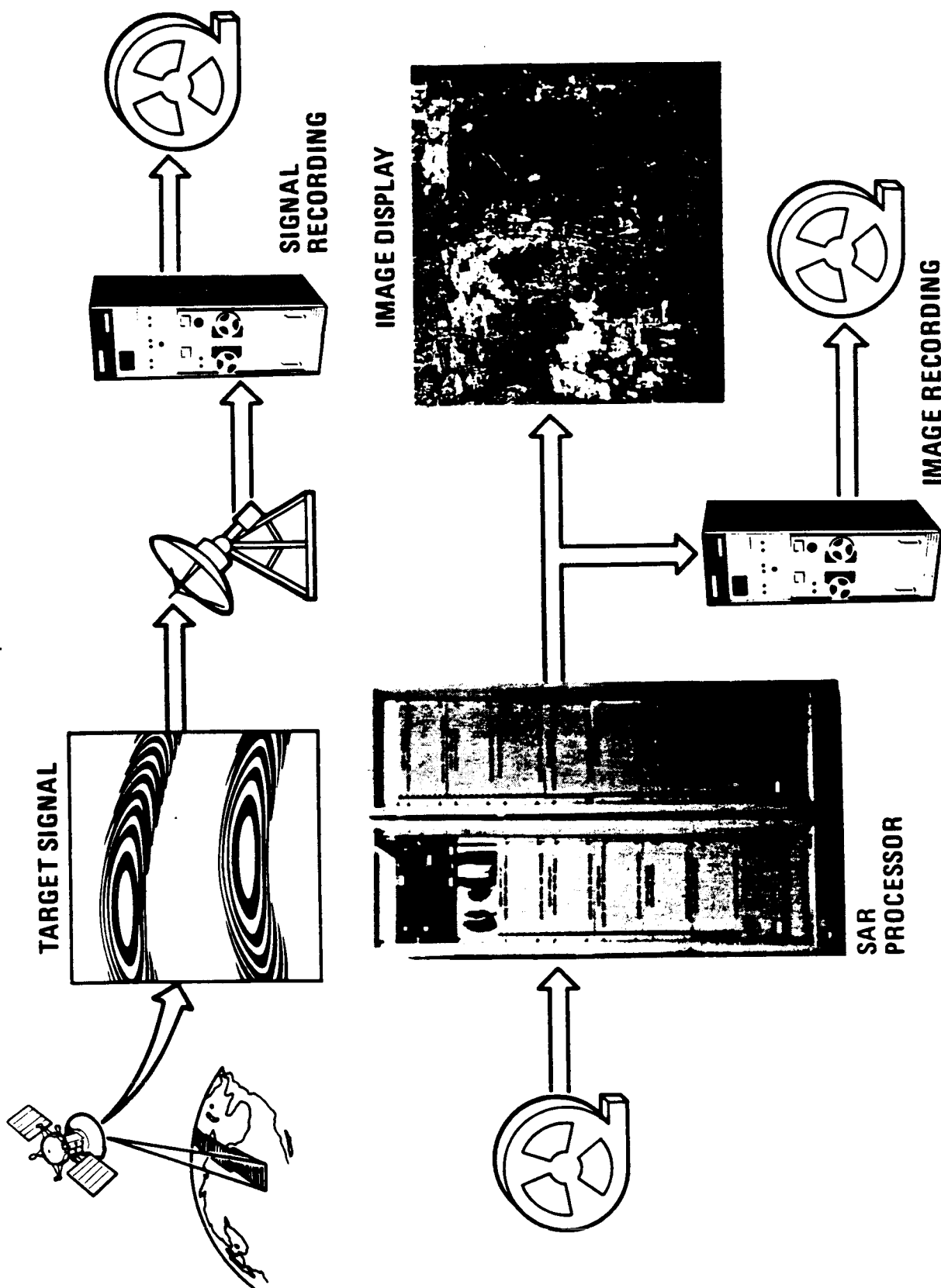
POINT TARGET
COMPRESSION OR FOCUSSING

RANGE CURVATURE

RANGE RESOLUTION

RANGE WALK

RANGE COMPRESSION
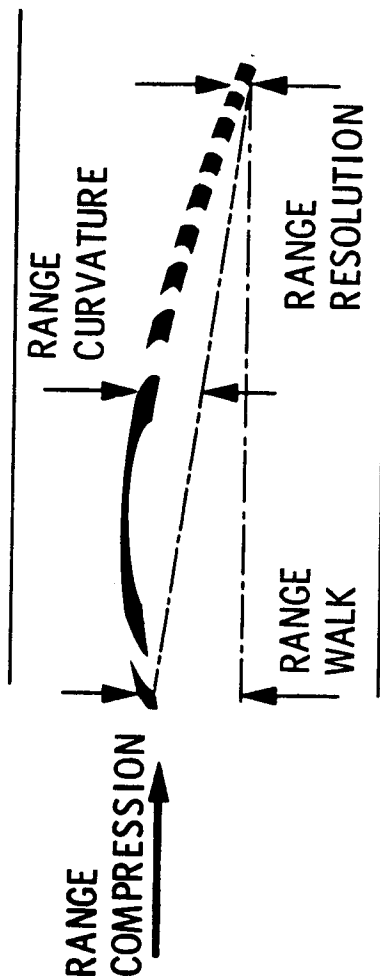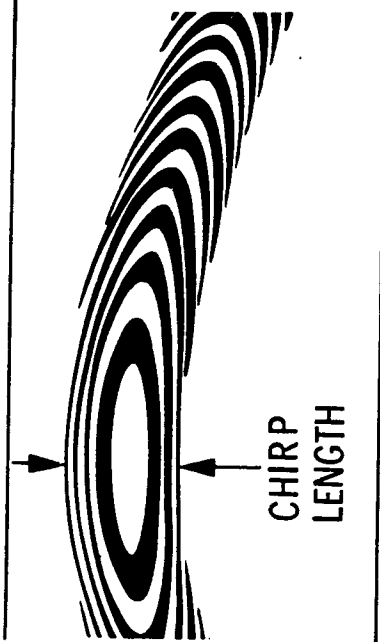
CHIRP LENGTH

$$\text{RANGE COMPRESSION RATIO} = \frac{\text{CHIRP LENGTH}}{\text{RANGE RESOLUTION}}$$

AZIMUTH RESOLUTION

AZIMUTH COMPRESSION

SINGLE LOOK APERTURE LENGTH

LOOK 1 | LOOK 2 | LOOK 3 | LOOK 4
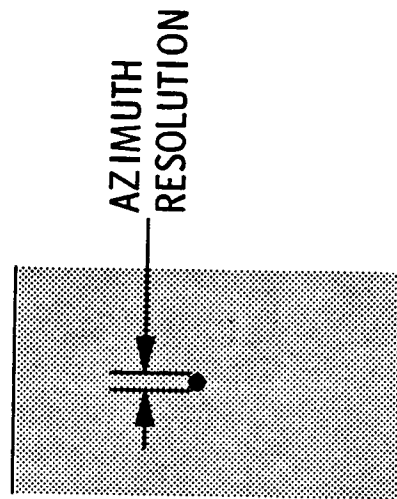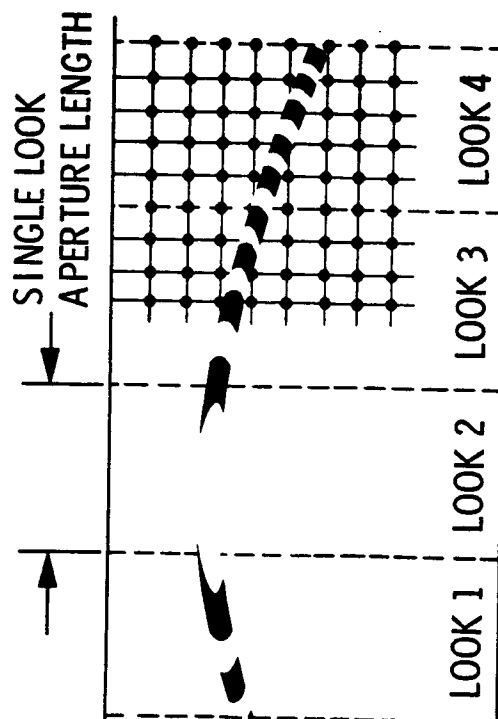
$$\text{AZIMUTH COMPRESSION RATIO} = \frac{\text{SINGLE LOOK APERTURE LENGTH}}{\text{AZIMUTH RESOLUTION}}$$

JPL

JPL

ADSP BACKGROUND

OBJECTIVES

● DEVELOP THE TECHNOLOGY REQUIRED TO MEET THE SAR PROCESSING NEEDS FOR MISSIONS IN THE LATE 1980's

● BUILD AND DEMONSTRATE A HIGH PERFORMANCE ENGINEERING MODEL FLEXIBLE ENOUGH TO BE EASILY ADAPTED TO A WIDE VARIETY OF SAR PROCESSING TASKS AND CAPABLE OF REAL-TIME OR NEAR REAL-TIME THROUGHPUT RATES

APPROACH

● IMPLEMENT SAR PROCESSING ALGORITHM ELEMENTS (FFT'S, MULTIPLIERS, MEMORY SYSTEMS, INTERPOLATORS, FUNCTION GENERATORS, ETC.) INTO A PROGRAMMABLE PIPELINE ARCHITECTURE

● USE ONLY COMMERCIALLY AVAILABLE INTEGRATED CIRCUITS TO MINIMIZE COST AND RISK

● OPTIMIZE ARCHITECTURE AND CIRCUIT DESIGN FOR THE BEST BALANCE OF TESTABILITY, FLEXIBILITY, AND EFFICIENCY

SAR MISSIONS AND PROCESSING SYSTEMS
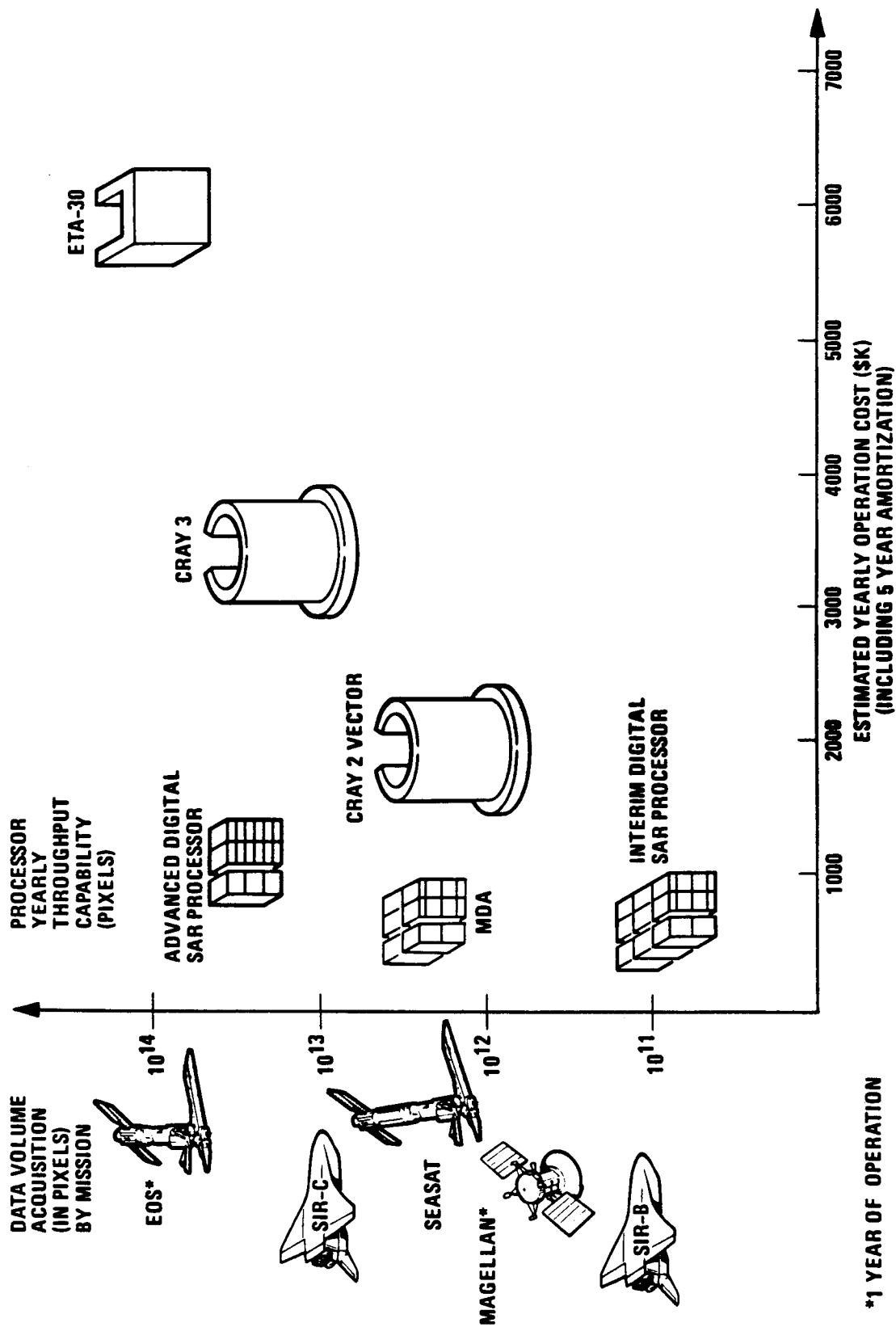
ADVANCED DIGITAL SAR PROCESSOR

SYSTEM DIAGRAM

INPUT HDR — INPUT INTERFACE — RANGE PROCESSOR — CORNER TURN MEMORY — AZIMUTH PROCESSOR — MULTI-LOOK PROCESSOR — OUTPUT INTERFACE — OUTPUT HDR

8086 μPROCESSOR

VAX-11/730 CONTROL COMPUTER
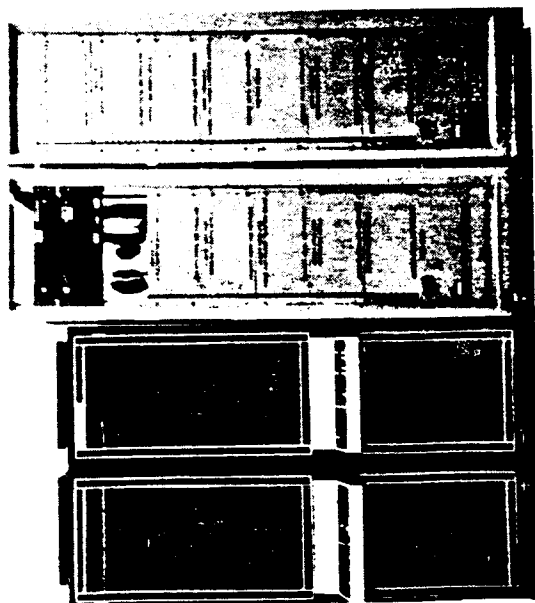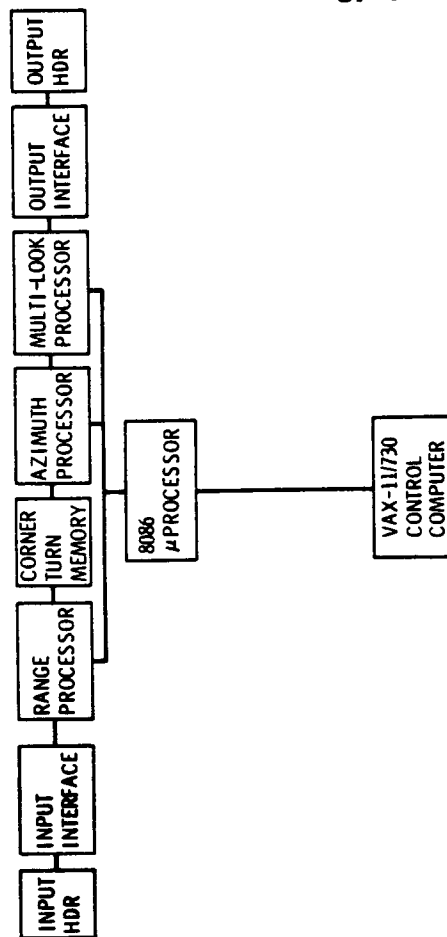
HDR & PROCESSOR

SIR-B IMAGE OF MONTREAL
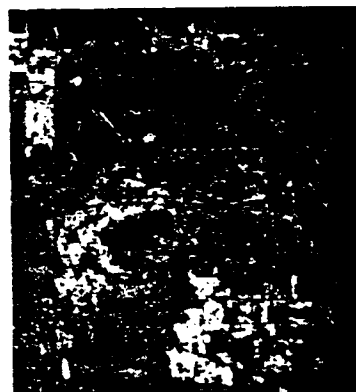
- STATE OF THE ART SAR PROCESSOR
- MORE THAN 6 GIGAFLOPS COMPUTE RATE
- OVER 150 MBYTES OF HIGH SPEED MEMORY
- SYSTEM WILL BE CORE PROCESSOR FOR FUTURE MISSIONS SUCH AS MAGELLAN, SIR, ERS-1, EOS

ADSP INTERFACE DIAGRAM

JPL
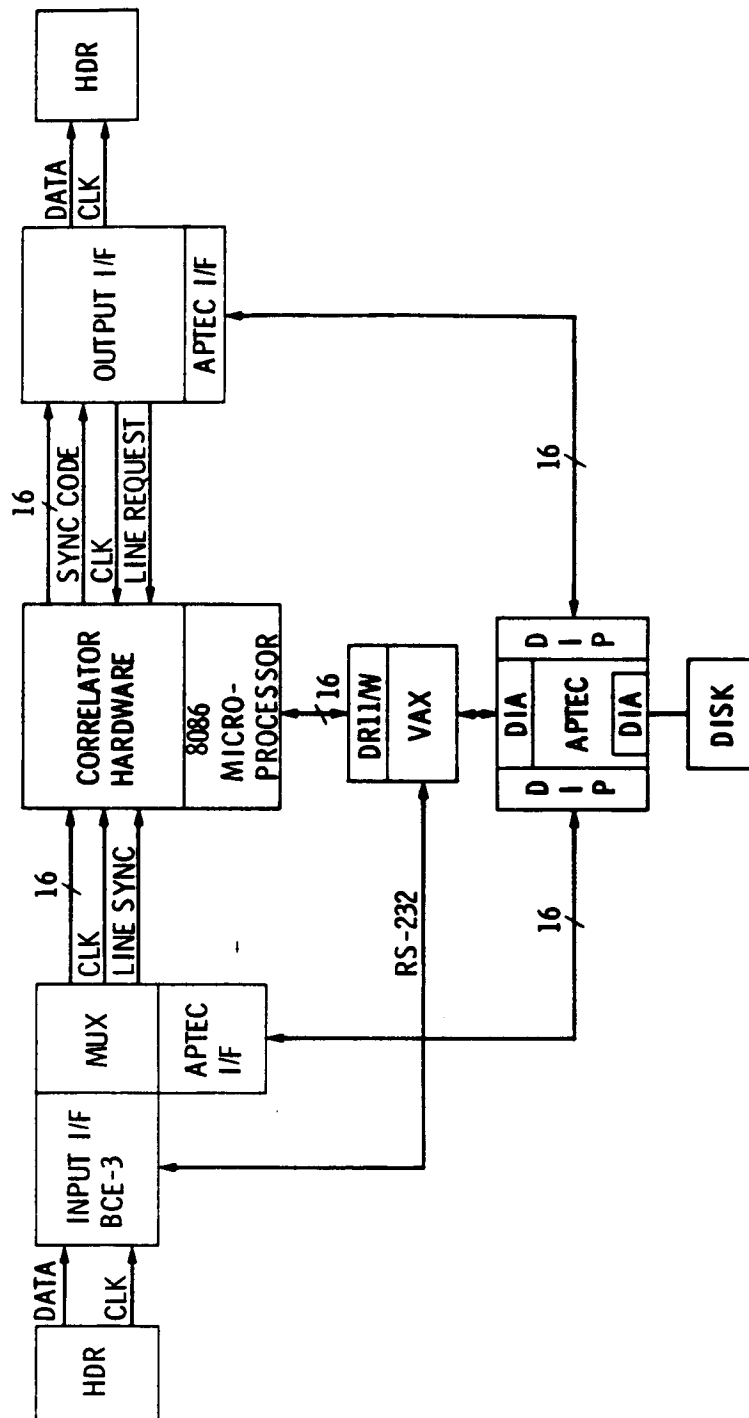
ADSP
MAJOR SUBSYSTEM SUMMARY

FFT MODULES (4 UNITS)

- 20 MHz PIPELINED FFT ($\sim$ 1.4 giga FLOPS)

- PROGRAMMABLE:

    REAL OR COMPLEX INPUT

    FORWARD OR INVERSE

    16 POINT TO 16K POINT LINE LENGTH

    CIRCULAR SHIFT

CORNER-TURN MEMORY

- 72 megabytes (24 bit WORDS)

- 30 mbytes/sec IN, 60 mbytes/sec OUT

- VARIABLE ASPECT RATIO, UP TO 8K LINE
  LENGTH IN RANGE OR AZIMUTH

JPL

ADSP
MAJOR SUBSYSTEM SUMMARY (Cont'd)

JPL

RANGE MIGRATION CORRECTION

- 24 megabytes

- 60 mbytes/sec IN, 240 mbytes/sec OUT

- 4 POINT INTERPOLATE (360 megaflops)

MULTI-LOOK MEMORY

- 48 megabytes

- 20 mbytes/sec IN, 20 mbytes/sec OUT

ADSP CORRELATOR HARDWARE

JPL
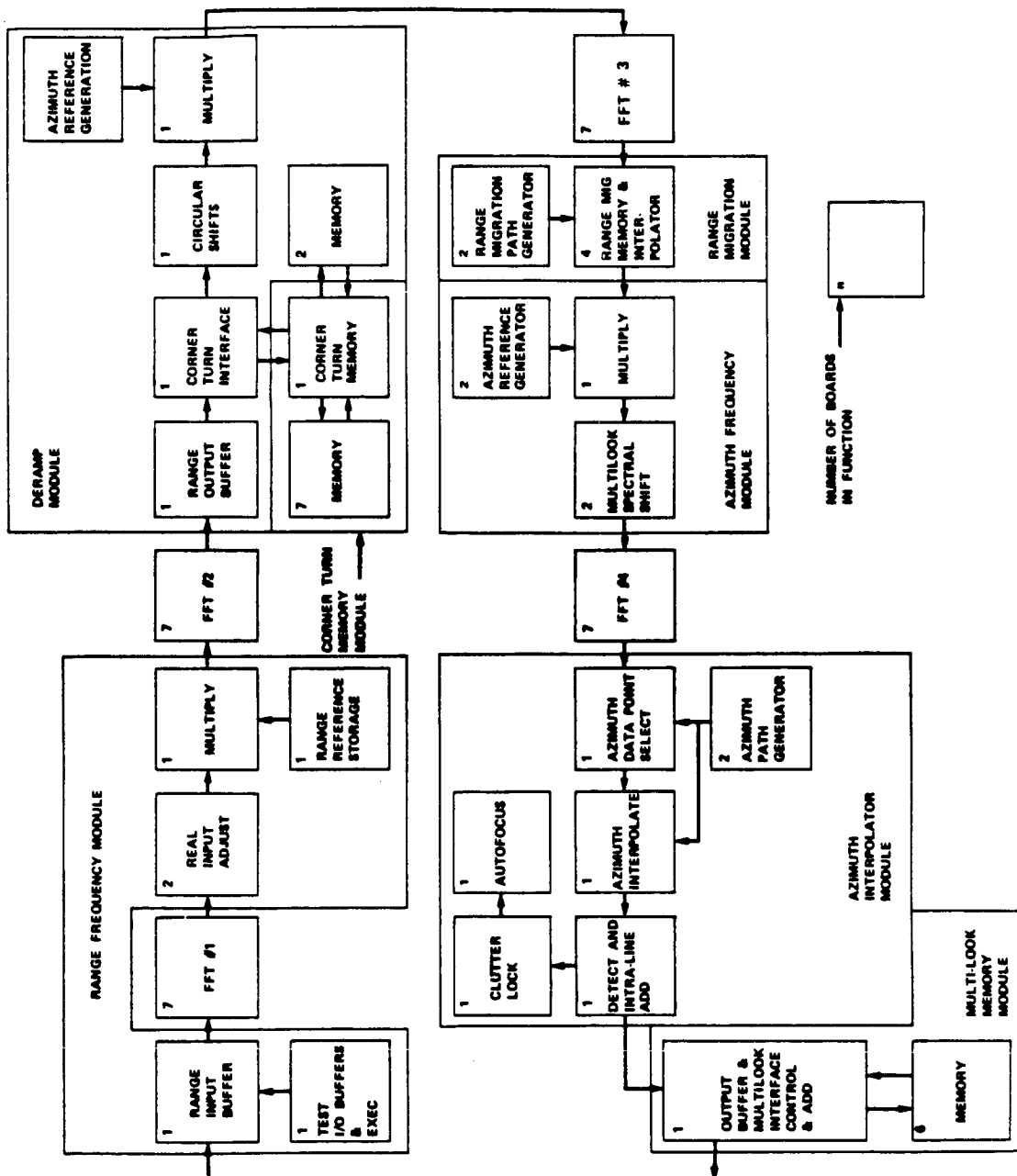
AZIMUTH PROCESSOR
FFT-CONVOLUTION ALGORITHM

JPL

RANGE
COMPRESSED
DATA
AZIMUTH
ORDER

FFT

RANGE
MIGRATION
CORRECTION

AZIMUTH
REFERENCE
GENERATOR

SPECTRUM
DIVISION
AND SHIFT

FFT^{-1}

AZIMUTH
INTERPOLATION

DETECT AND
INTRA-LINE
ADD

MULTI-LOOK
AND
CORNER-TURN
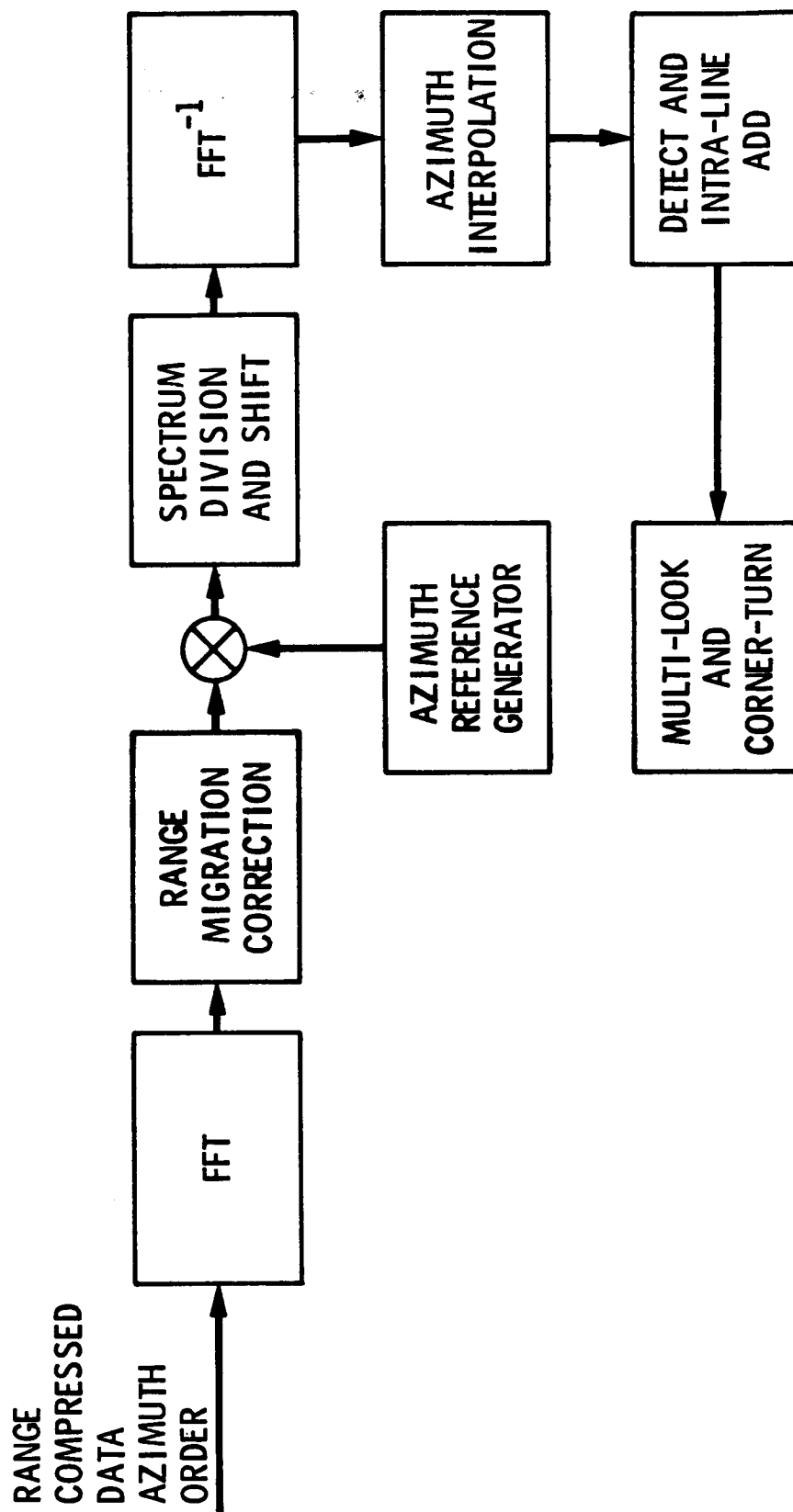
AZIMUTH PROCESSOR
DERAMP-FFT ALGORITHM

JPL

RANGE
COMPRESSED
DATA
AZIMUTH
ORDER

AZIMUTH
REFERENCE
GENERATOR

FFT

RANGE
INTERPOLATION

AZIMUTH
INTERPOLATION

MULTI-LOOK
AND
CORNER-TURN
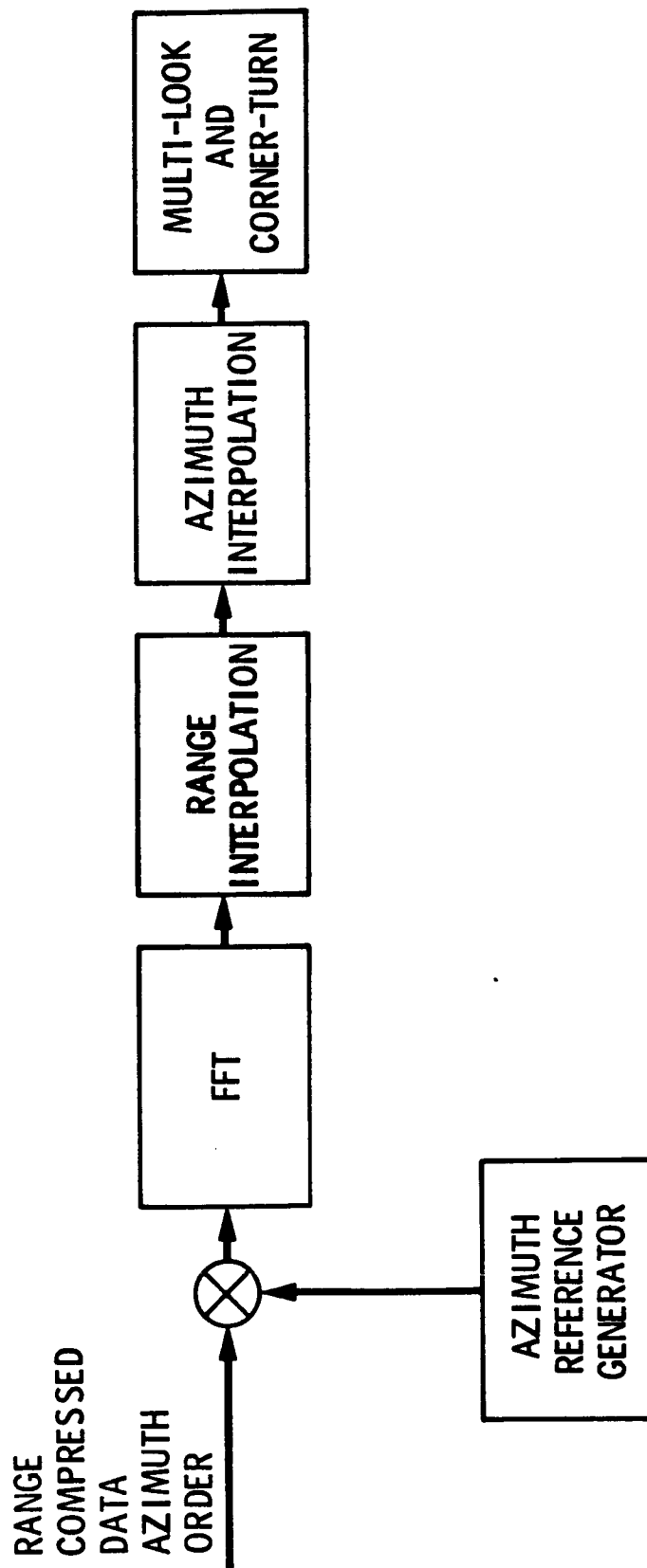
RANGE MIGRATION INTERPOLATION
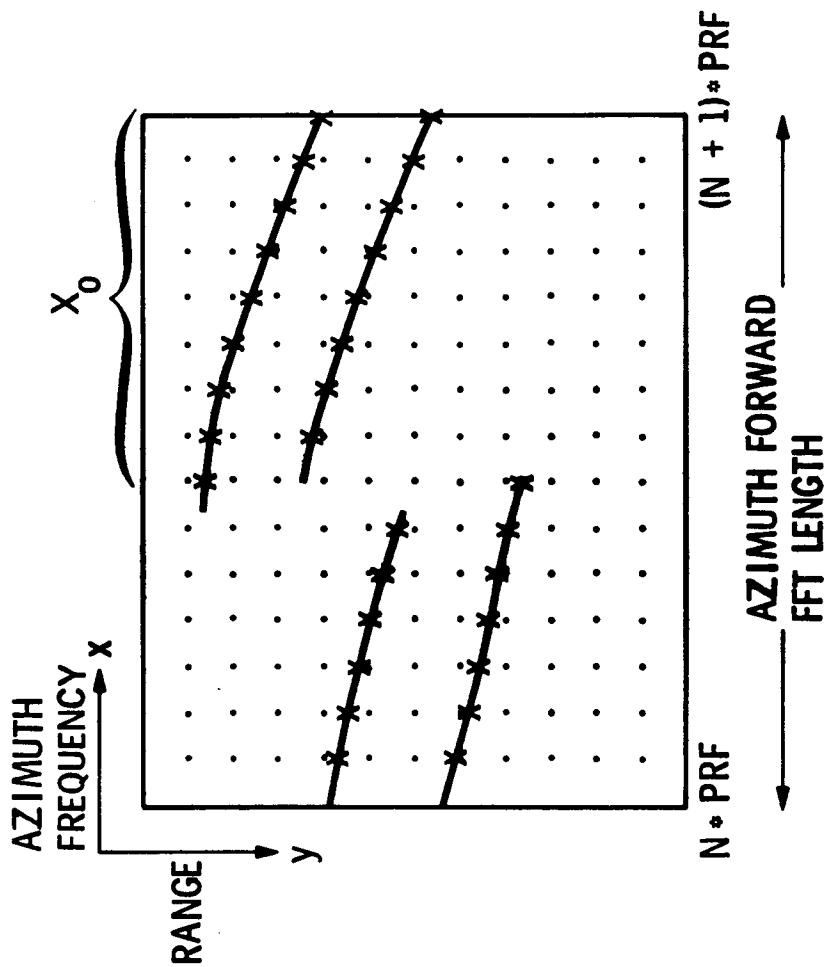
$$P(x, y) = a(y) (x + x_0(y))^2 + b(y) (x + x(y)) + x(y)$$

$$\text{GENERAL FORM} \quad f(y) = f_2 y^2 + f_1 y + f_0$$

$$(x + x_0) \text{ IS MODULE FFT}$$

$P(x, y)$ IS RANGE POSITION (OFFSET) OF THE DESIRED OUTPUT SAMPLE RELATIVE TO CURRENT INPUT SAMPLE

ADSP PIPELINE FUNCTIONS

44 ∓ 20 MHz

RANGE MIGRATION INTERPOLATION
8 MWORDS
(24 BIT)
4 POINT
INTERPOLATE
2-D QUADRATIC
PATH (ADDRESS)
GENERATOR
300 MBYTE/S
INTERNAL I/O
360×10^6 FLOPS

AZIMUTH REFERENCE GENERATOR
e^{iax^2}

DERAMP REFERENCE MULTIPLY ⊗

FFT

44 ∓ 20 MHz

CORNER-TURN MEMORY
24 MWORDS
(24 BIT)
9, 9, 6 FORMA

24 ∓ 10 MHz

BUFFER

44 ∓ 20 MHz

FFT⁻¹

AZIMUTH REFERENCE MULTIPLY ⊗ e^{iax^2}

MULTI-LOOK SPECTRAL PARTITION

FFT⁻¹

REFERENCE FUNCTION MEMORY → ⊗

FFT
UP TO
16K COMPLE
1.4×10^9 FLOPS

AZIMUTH INTERPOLATION
PATH
GENERATOR
4 POINT
INTERPOLATE

20 MHz
SYNCHRONOUS
22I, 22Q

CLUTTER-LOCK ACCUMULATOR

AUTOFOCUS CROSS-CORRELATOR

DETECT

16 ∓ 20 MHz

INTR-LINE ADD

16 ∓ 10 MHz

MULTI-LOOK MEMORY
24 MWORD
(16 BIT)
INTER-FRAME
ADD

SYNCHRONIZER BUFFER

∓ 44

UP TO 10 MHz
ASYNCHRONOUS
8I, 8Q

- OVER 6×10^9 FLOPS
- 28,000 LSI AND VLSI IC'S
- 150 MBYTES FAST MEMORY
- 75 BOARDS, 12 KW POWER

16 ∓

RANGE ORDER INTENSITY
ASYNCHRONOUS UP TO
10 MHz

2-261

ADVANCED DIGITAL SAR PROCESSOR

STATUS

ENGINEERING MODEL COMPLETED

- CORRELATOR: 25 BOARD DESIGNS, DIAGNOSTICS, 75 TOTAL BOARDS, 28,000 IC'S, 12 KW POWER

- CONTROL COMPUTER: VAX 11/730 WITH SYSTEM TEST SOFTWARE (~ 5000 LINES OF CODE)

- I/O INTERFACES: APTEC AND HDDT INPUT, APTEC AND SCROLLING DISPLAY OUTPUT

DEMONSTRATED PERFORMANCE

- MORE THAN 6 GIGAFLOP COMPUTE RATE USING POINT TARGET TEST PATTERNS

- PROCESSED SIR-B DATA INTO IMAGERY AT 50 MBITS/SEC INPUT RATE (1.5 TIMES REAL-TIME RATE) IN BOTH BURST MODE (MAGELLAN) AND CONTINUOUS MODE (SIR)

JPL

ADVANCED DIGITAL SAR PROCESSOR

APPLICATIONS

MISSION	STATUS	APPROACH
MAGELLAN	COMMITTED	WILL USE ORIGINAL ADSP AT 1/4 CAPACITY
SIR-C	COMMITTED	WILL USE ORIGINAL ADSP AT FULL CAPACITY
ALASKA SAR FACILITY • ERS-1 • JERS-1 • RADARSAT	COMMITTED	JPL WILL BUILD VERSION OF ADSP
EOS SAR	IN PLANNING	NEXT GENERATION ADSP / ON-BOARD PROCESSOR
AIRCRAFT SAR	IN PLANNING	WOULD USE ORIGINAL ADSP

NASA COMPUTER SCIENCES AND DATA SYSTEMS WORKSHOP

FLIGHT SAR PROCESSOR STUDY

W. Arens

JPL

November 1986

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL

FLIGHT SAR PROCESSING

- LONG-TERM OBJECTIVE

  - TO DEFINE AND DEVELOP THE ENABLING TECHNOLOGY REQUIRED FOR SAR IMAGE GENERATION ONBOARD EOS-TYPE MISSIONS

- RATIONALE

  - REDUCES ON-BOARD DATA HANDLING AND STORAGE REQUIREMENTS

  - ALLOWS ON-BOARD INSTRUMENT AUTONOMY AND CONTROL

  - REDUCES DOWNLINK DATA TRANSFER REQUIREMENTS

  - REDUCES GROUND PROCESSING AND OPERATIONS REQUIREMENTS

  - ALLOWS DIRECT DISSEMINATION OF INFORMATION TO USERS

STUDY BACKGROUND

JPL

- INITIATED AS FLIGHT ARRAY PROCESSOR STUDY (FY '84)

  • GENERAL PURPOSE SIGNAL PROCESSING

  • EXCESSIVE POWER AND MASS FOR SAR WITH PROJECTED TECHNOLOGY

- CHANGED TO FLIGHT SAR PROCESSOR STUDY (FY '86)

  • SPECIAL PURPOSE SAR PROCESSING

  • POTENTIALLY ACCEPTABLE POWER AND MASS WITH EXISTING TECHNOLOGY

STUDY OBJECTIVE

JPL

- TO DETERMINE THE FEASIBILITY OF IMPLEMENTING A PRACTICAL FLIGHT SAR PROCESSOR FOR NEAR-TERM EOS-TYPE APPLICATIONS

JPL   FY '86 TECHNICAL APPROACH

- DEFINE THE PRELIMINARY FUNCTIONAL REQUIREMENTS FOR AN EOS FLIGHT SAR PROCESSOR

- DEFINE A PRELIMINARY BASELINE PROCESSOR DESIGN ARCHITECTURE TO MEET THE FUNCTIONAL REQUIREMENTS

- ASSESS THE IMPLEMENTATION AND TECHNOLOGY NEEDS FOR THE BASELINE PROCESSOR

- PROPOSE A STRAWMAN DEVELOPMENT STRATEGY FOR THE BASELINE PROCESSOR

- ESTIMATE PROCESSOR POWER, MASS, AND RISK FOR EOS-TYPE MISSION APPLICATIONS

JPL

PROCESSING REQUIREMENTS

- ACCOMMODATE THREE RADAR RECEIVER FREQUENCY CHANNELS (L, C, AND X) EACH PROVIDING 100 MBPS OF MULTI-POLARIZED DATA

- PROCESS DATA FROM ONE 100 MBPS CHANNEL INTO IMAGES IN REAL TIME WHEN RADAR ON

- SEQUENTIALLY PROCESS DATA FROM REMAINING 100 MBPS CHANNELS INTO IMAGES WHEN RADAR OFF (RADAR DUTY CYCLE $\approx$ 20%)

- PROVIDE 4-LOOK IMAGES AT 30-METER RESOLUTION OVER A 100 KM SWATH

JPL BASELINE ARCHITECTURE DEFINITION

GOAL

DEFINE A PRACTICAL FLIGHT SAR PROCESSOR ARCHITECTURE FOR EOS-TYPE MISSIONS

THE PROBLEM

ON-BOARD SAR IMAGE GENERATION

THE SOLUTION

A VLSI CHIP TAILORED TO AZIMUTH PROCESSING NEEDS

CAPABILITY

>5:1 REDUCTION IN DATA RATE AND VOLUME

RELIABILITY

- EASY TO REPLACE OR SPARE CHIPS
- GRACEFUL PERFORMANCE DEGRADATION

RAW SAR DATA

INPUT PROCESSING

RANGE PROCESSING

AZIMUTH PROCESSING

VAC 1

VAC 2

VAC N

MUX

OUTPUT PROCESSING

IMAGES

THE ARCHITECTURE

- PARALLEL CHIPS
- NO BULK MEMORY
- SAME INPUT TO ALL CHIPS
- SEQUENTIAL READOUT OF CHIPS

VLSI AZIMUTH CHIP

- PRODUCES IMAGE LINES
- INDEPENDENT OF OTHER CHIPS
- FULLY PROGRAMMABLE

AZIMUTH PROCESSING

ARCHITECTURE

- IDENTICAL PIPELINED PROCESSING CHANNELS IN PARALLEL
- UNIQUE IMAGE LINES FROM EACH CHANNEL
- SEQUENTIAL READOUT OF CHANNELS

IMPLEMENTATION

- VLSI AZIMUTH CHIPS
- ONE OR MORE CHANNELS PER CHIP
- LOW POWER AND MASS

INTERPOLATED RANGE LINES

RANGE MIGRATION CORRECTION COEFFICIENTS D_1-D_N

AZIMUTH REFERENCE FUNCTION COEFFICIENTS C_1-C_N

GATE 1   GATE 2   GATE N

ACC 1   ACC 2   ACC N

OUTPUT MULTIPLEXER

IMAGE LINES

JPL

JPL   AZIMUTH PROCESSOR FEATURES

- A PIPELINED PROCESSING CHANNEL INDEPENDENTLY PRODUCES IMAGE LINES

- REAL-TIME PROCESSING ACHIEVED BY PARALLELING CHANNELS

- NO DATA TRANSFER REQUIRED BETWEEN CHANNELS

- SINGLE INPUT LINE TO ALL CHANNELS

- ALL CHANNEL OUTPUTS MULTIPLEXED INTO A SINGLE OUTPUT LINE

- PRECISE RANGE MIGRATION CORRECTION

- PROGRAMMABLE AZIMUTH CORRELATION

- NO BULK MEMORY REQUIREMENTS

- GRACEFUL PERFORMANCE DEGRADATION

JPL

FY'86 RESULTS

- PROCESSOR FUNCTIONAL REQUIREMENTS DEFINED

- BASELINE PROCESSOR DESIGN ARCHITECTURE DEFINED

- IMPLEMENTATION AND TECHNOLOGY NEEDS ASSESSED

  - CURRENT CMOS VLSI CHIP TECHNOLOGY ADEQUATE

- DEVELOPMENT STRATEGY PROPOSED

  - 9-YEAR, $20 M PROGRAM THROUGH FLIGHT PROTOTYPE

  - TWO FIRST-YEAR HARDWARE DEVELOPMENT TASKS

- EOS IMPLEMENTATION CHARACTERISTICS ESTIMATED

  - POWER ≈ 500 WATTS

  - MASS ≈ 100 KILOGRAMS

  - LOW RISK BASED ON CONSERVATIVE ESTIMATES

JPL

FY '86 CONCLUSION

- FLIGHT SAR PROCESSING FOR NEAR-TERM EOS-TYPE MISSIONS APPEARS FEASIBLE

- EXISTING SPACE QUALIFIABLE TECHNOLOGY IS APPLICABLE

- MASS AND POWER REQUIREMENTS ARE REASONABLE

- DEVELOPMENT TIME IS COMPATIBLE WITH EOS OPPORTUNITY

FY '86 DELIVERABLES

JPL

- PRELIMINARY FUNCTIONAL REQUIREMENTS DOCUMENT

- PRELIMINARY BASELINE DESIGN DESCRIPTION DOCUMENT

- FY '86 RTOP REPORT

  - PROCESSING NEEDS ASSESSMENT

  - ARCHITECTURE CHARACTERISTICS DEFINITION

  - IMPLEMENTATION NEEDS ASSESSMENT

  - AZIMUTH PROCESSOR TRADEOFF STUDY

  - BASELINE ARCHITECTURE DEFINITION

  - TECHNOLOGY NEEDS ASSESSMENT

  - DEVELOPMENT STRATEGY

JPL

FY '87 PLAN

- REFINE FLIGHT SAR PROCESSOR PERFORMANCE REQUIREMENTS

- DEVELOP OPERATIONAL SCENARIOS FOR EOS-TYPE MISSIONS

- DEVELOP COST TRADEOFFS FOR FLIGHT SAR PROCESSING

- PERFORM PROCESSOR DESIGN TRADEOFFS AT THE SYSTEM LEVEL

- REFINE DEVELOPMENT STRATEGY FOR FLIGHT PROTOTYPE PROCESSOR

- CONDUCT PERIODIC PEER-LEVEL DESIGN REVIEWS

- UPDATE FUNCTIONAL REQUIREMENTS AND DESIGN DESCRIPTION DOCUMENTS

ELECTRONIC ASSOCIATIVE MEMORY BASED ON HOPFIELD'S NEURAL NETWORK MODEL

Anil Thakoor

ADVANCED ELECTRONIC MATERIALS
AND DEVICES SECTION

JPL

Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL

UNIQUE FEATURES OF
NEURAL NETWORK MEMORY

- **ULTRA HIGH DENSITY:** ~ 10^9 BITS/CM^2

- **ELECTRONIC INPUT/OUTPUT:** NO MOVING PARTS

- **MEMORY NON-VOLATILE:** RADIATION RESISTANT

- **MEMORY DISTRIBUTED IN 'PASSIVE' INTERCONNECTIONS (SYNAPSES):**
  : LARGE STORAGE CAPACITY (10^2-10^4 BITS) PER ACTIVE DEVICE, (TRANSISTOR)

- **ASSOCIATIVE NATURE:**

- **CONTENT ADDRESSABILITY:** RETRIEVAL FROM PARTIAL INPUT

- **FAULT-TOLERANCE:** RETRIEVAL FROM PARTIALLY INCORRECT INPUT:
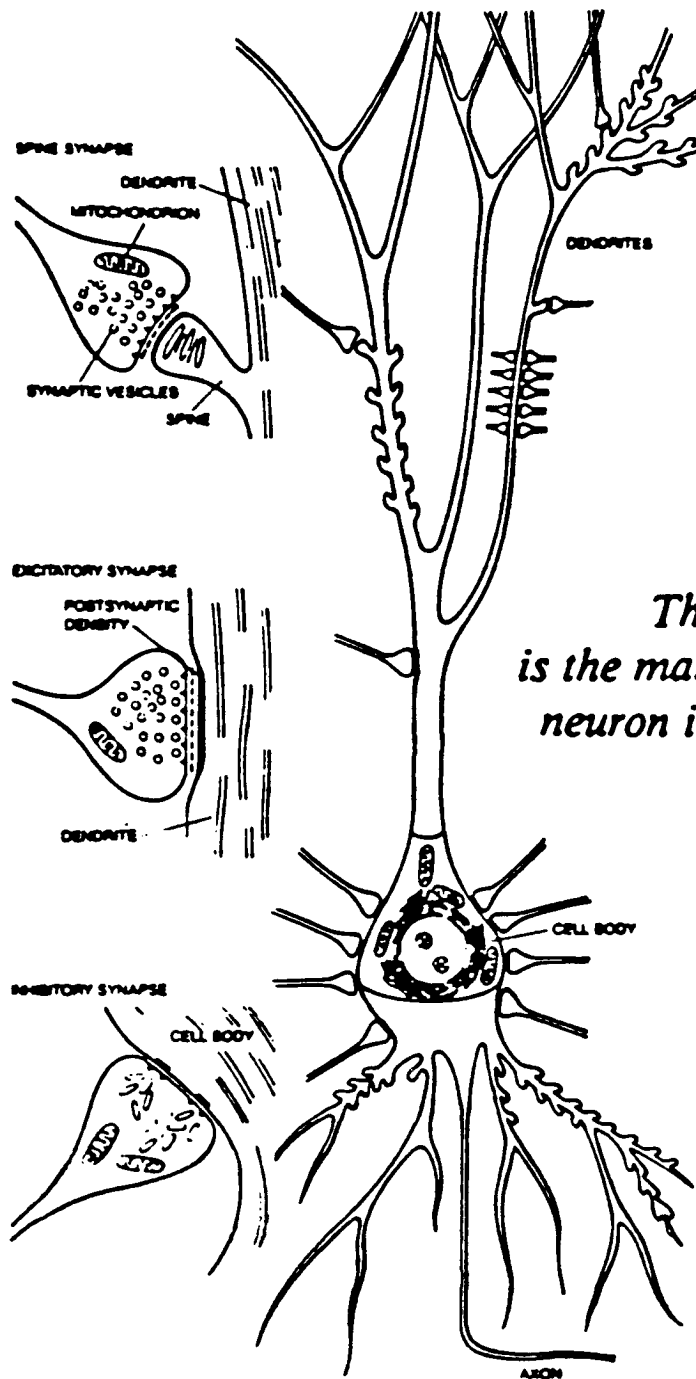 : ALSO, NO LOSS OF INFORMATION BY LOSS OF SOME CONNECTIONS
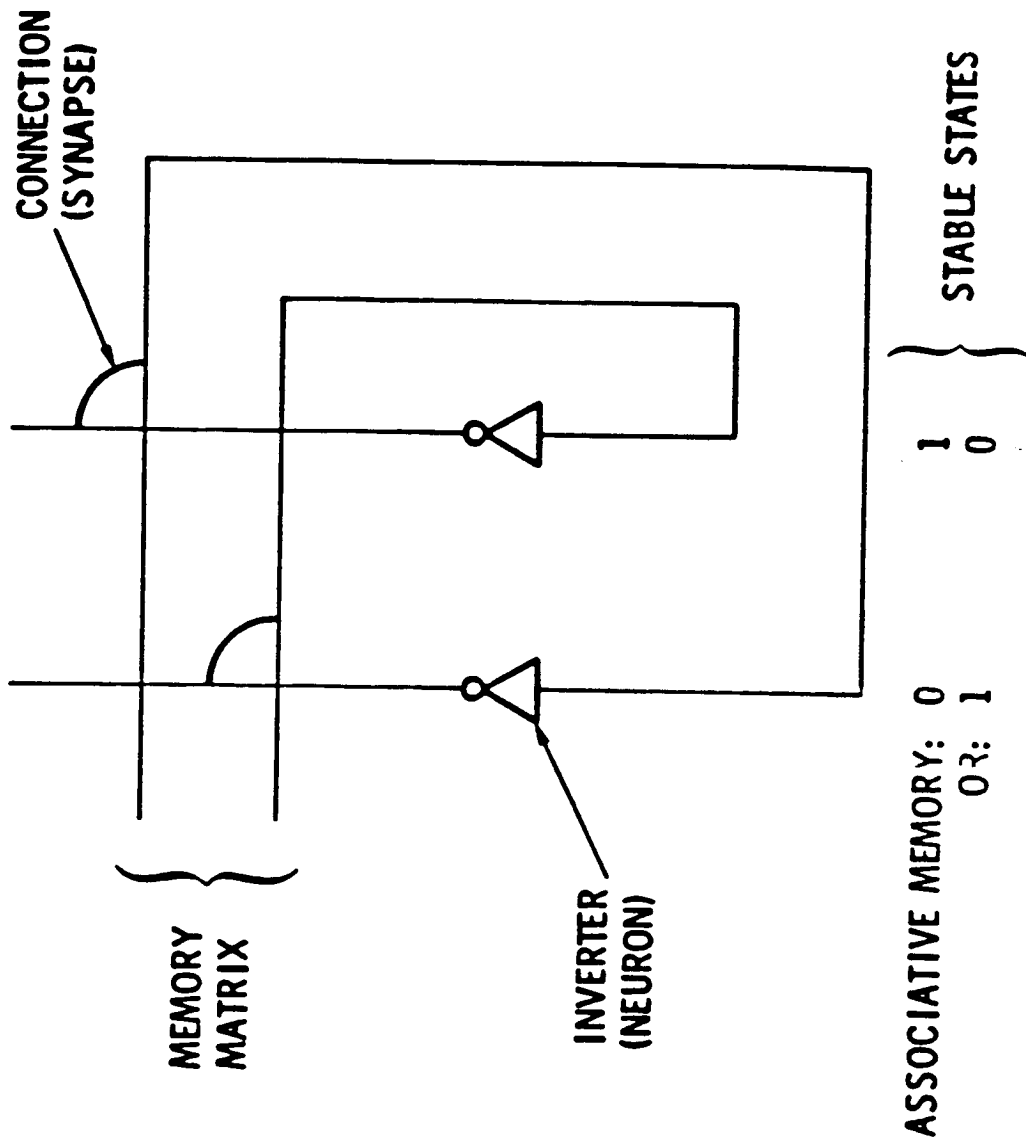
THE GRAY MATTER

JPL
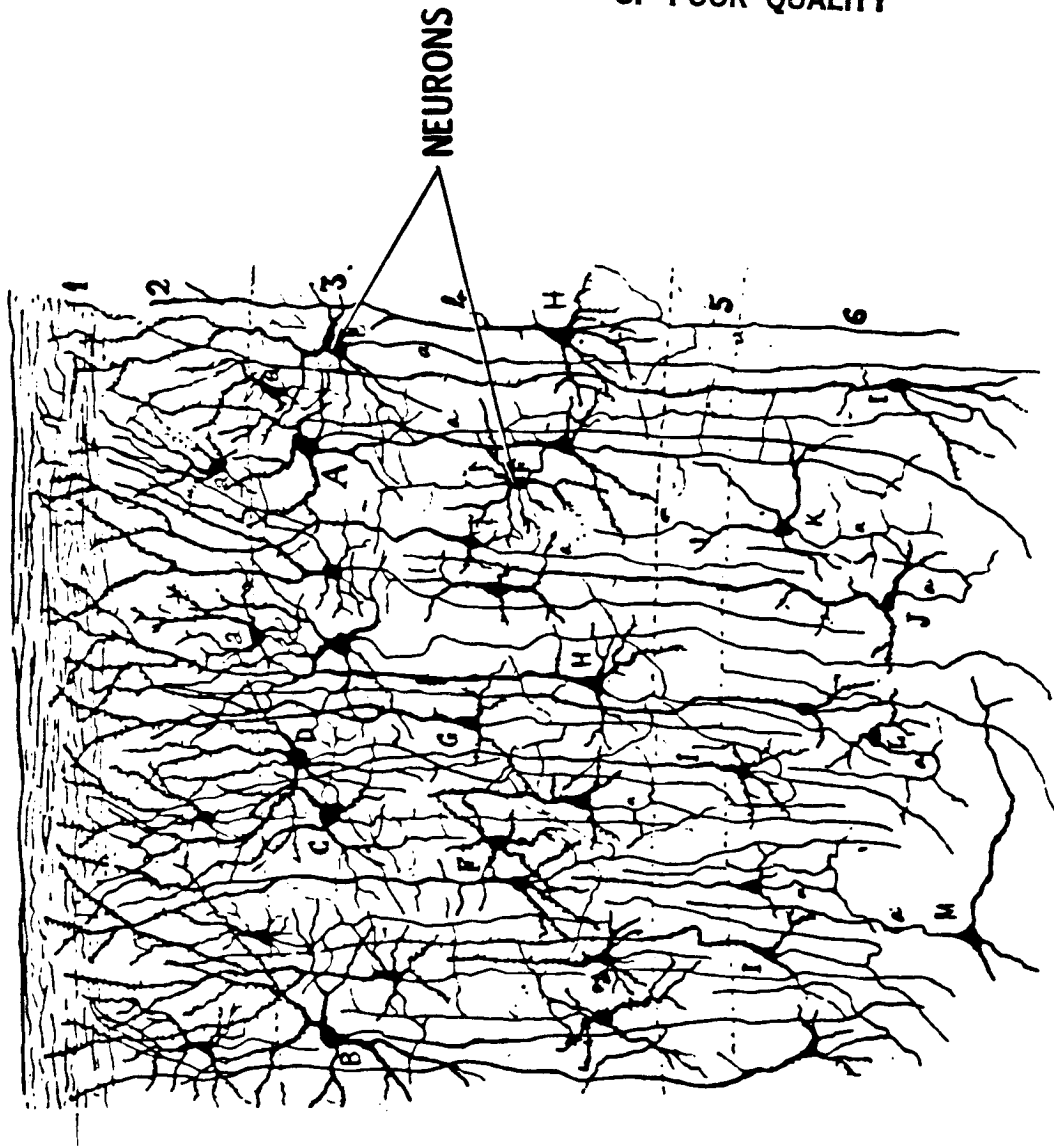
How Does the Brain Learn?

*The pyramidal cell
is the main type of output
neuron in the cortex and
hippocampus.*

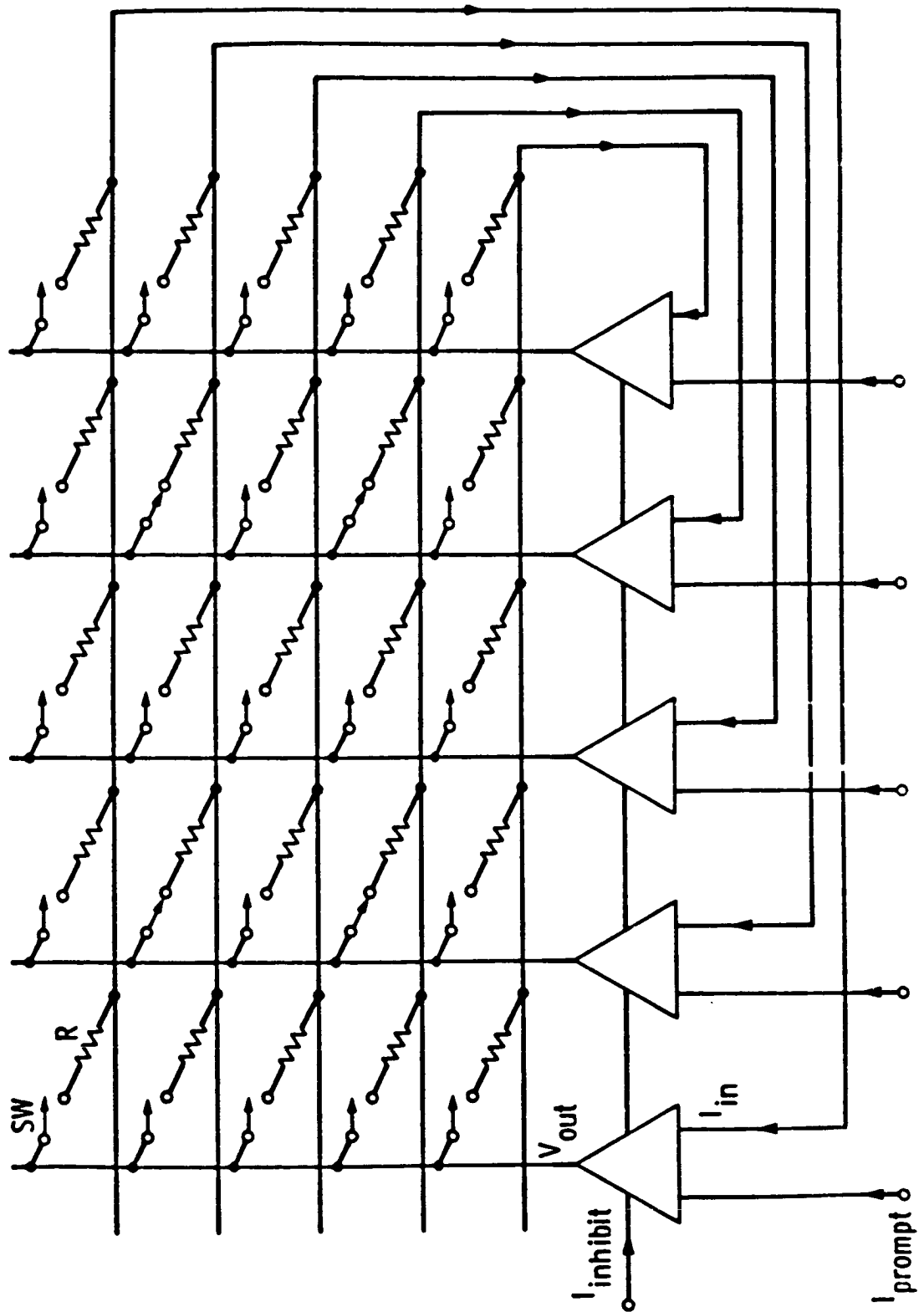# OUTLINE

- WHAT IS A NEURAL NETWORK?

  HOW DOES IT WORK?

- WHY ELECTRONIC NEURAL NETS?

  WHAT DO THEY PROMISE?

- JPL's RESEARCH APPROACH

  WHERE ARE WE TODAY?

- FUTURE PLANS

  WHERE ARE WE GOING?

JPL

A FLIP FLOP CIRCUIT

JPL

CONNECTION
(SYNAPSE)

MEMORY
MATRIX

INVERTER
(NEURON)

ASSOCIATIVE MEMORY: 0
OR: 1

1
0
} STABLE STATES

2-282

CONNECTION MATRIX MEMORY

JPL   'NEURON' DEVICE CHARACTERISTICS

$$I^i_{in} \sim \sum_j T_{ij} \, v^j_{out} + i^i_{prompt}$$

$$I^i_{inhibit} \sim \sum_j v^j_{out}$$

JPL
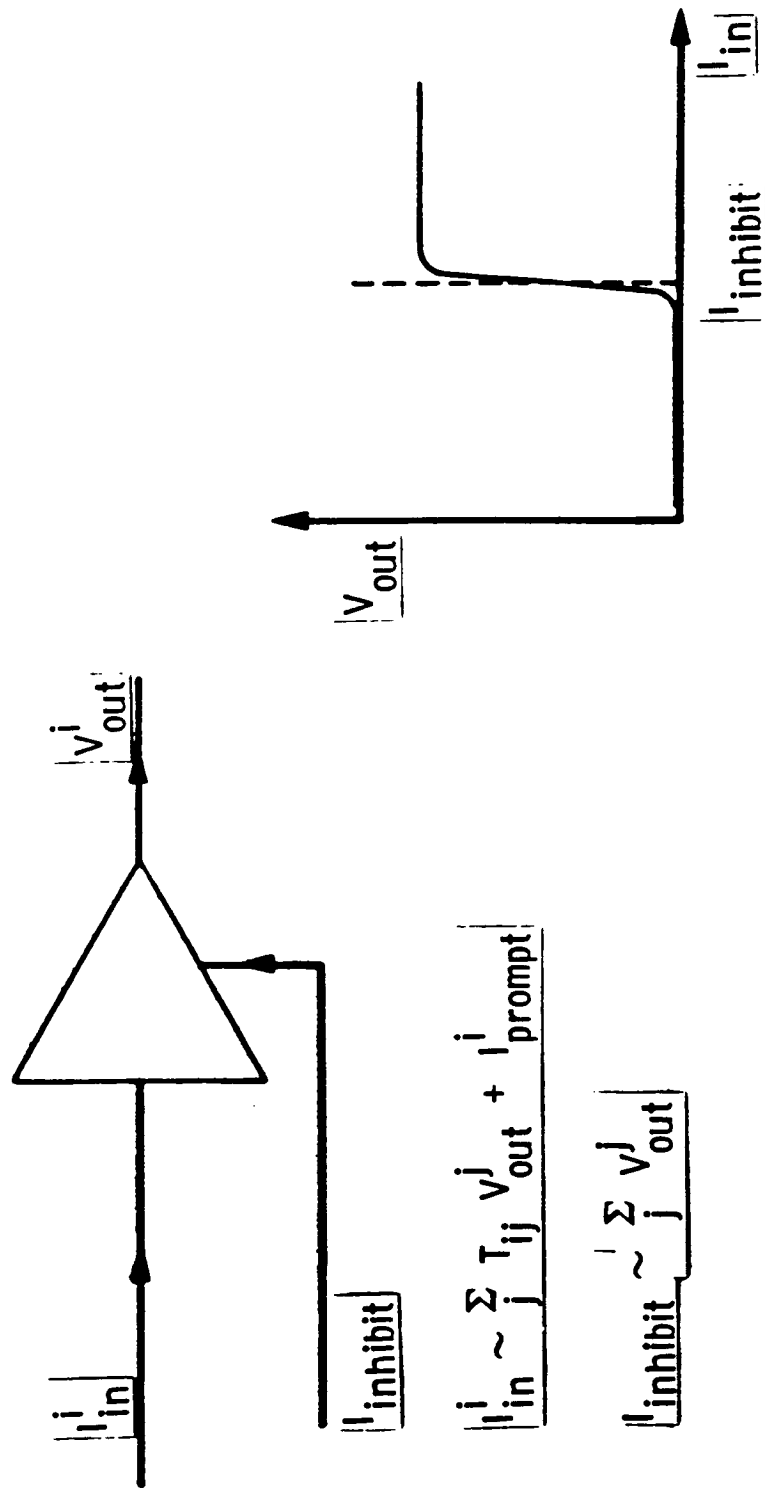
BINARY MEMORY MATRIX CONCEPT

- HOPFIELD MODEL (HOPFIELD, 1982)

  CONNECTION STRENGTH

  $$T_{ij} = \begin{cases} \sum_s (2V_i^s - 1)(2V_j^s - 1), & i \neq j \\ 0, & i = j \end{cases}$$

- BINARY MEMORY MATRIX
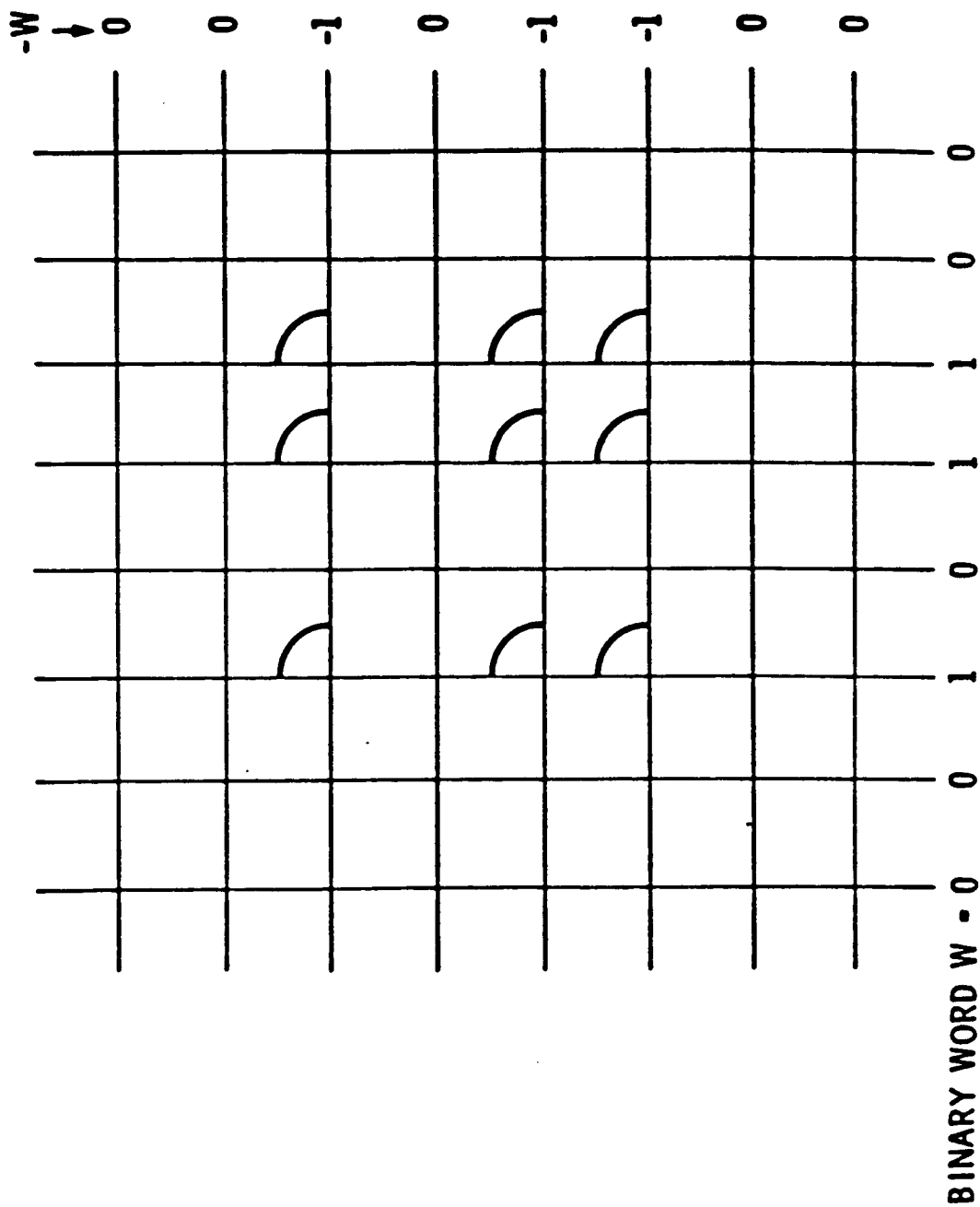
  $$\bullet \; T_{ij} = \begin{cases} 1 \text{ IF } \sum_s V_i^s V_j^s > 0 \\ 0 \text{ OTHERWISE} \end{cases}$$

OUTER PRODUCT WRITING PROCESS
AUTO ASSOCIATIVE MODE

JPL

BINARY WORD W = 0

WRITING PROCESS
"TAPE-RECORDER" MODE

JPL

WORD V

1 0 0 0 1 0 1 0

WORD U = 0

C-4

HIGH DENSITY, ELECTRONIC ASSOCIATIVE REFLEX MEMORY

JPL

LINE BY LINE, PARALLEL READOUT

INPUT (DRIVE)

PARALLEL OUTPUT

BINARY MEMORY MATRIX
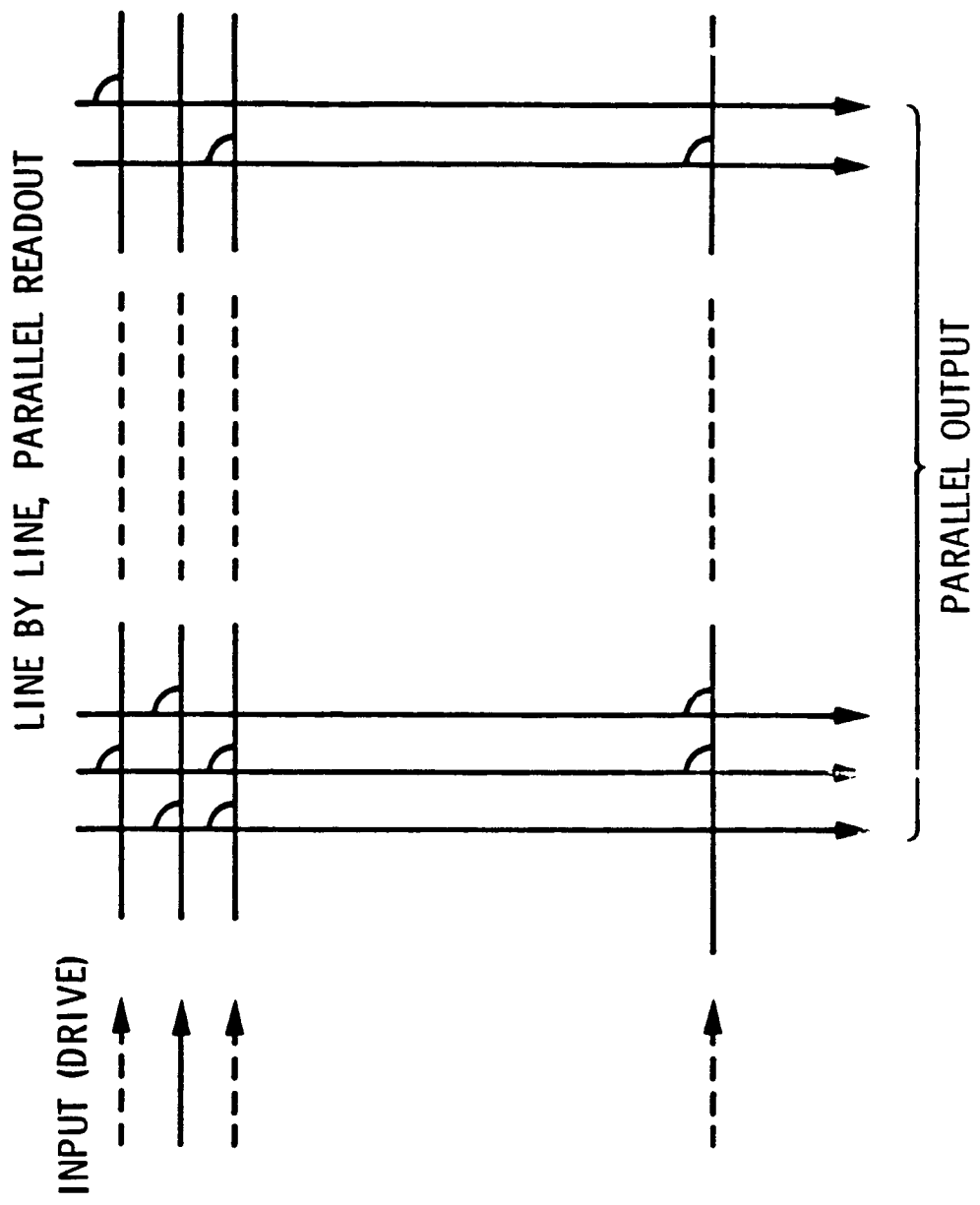
SERIAL-IN/PARALLEL-OUT
SHIFT REGISTERS

SWITCH
CONTROL
BITS IN

SW11 SW12 SW13 SW14

SW21 SW22 SW23 SW24

SW31 SW32 SW33 SW34

SW41 SW42 SW43 SW44

SWiJ

R

i

J

JPL
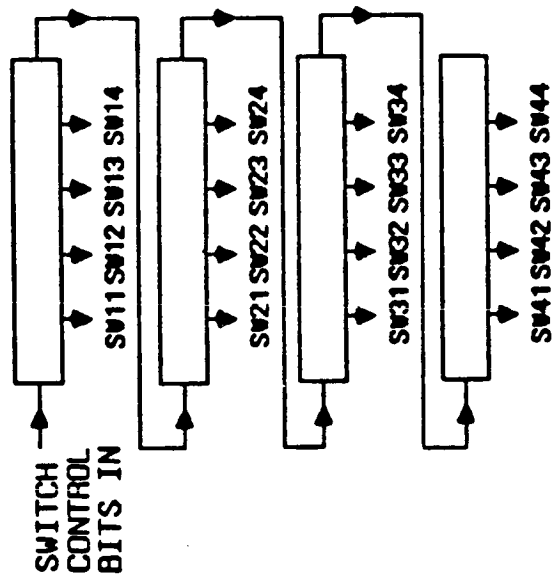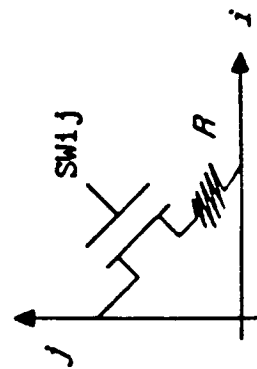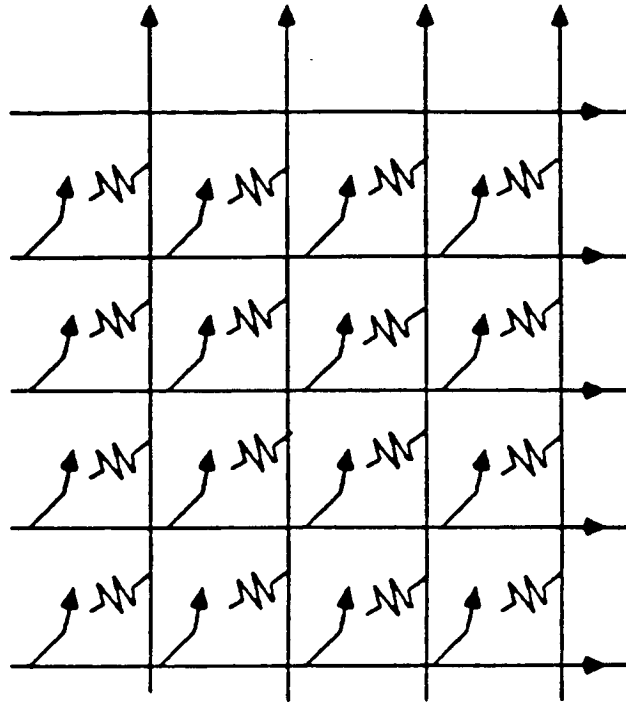
BINARY MEMORY MATRIX SYSTEM FOR NEURAL NETWORK SIMULATION

SAMPLE NAME RECALL FROM THE PROGRAMMABLE 32x32 BINARY MATRIX MEMORY

JPL

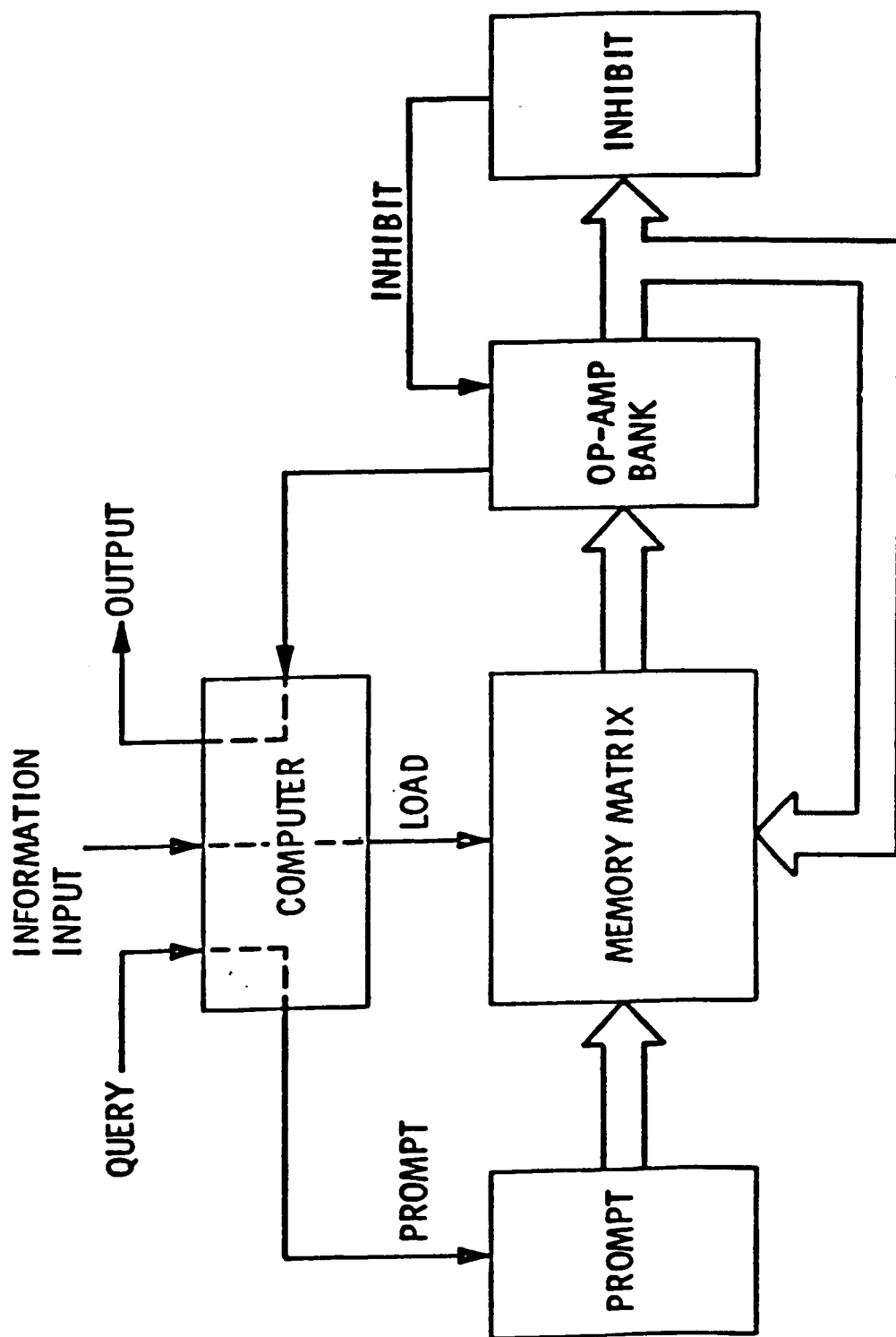| STORED NAME	BINARY CODE	PROMPT	MEMORY OUTPUT
JANE	01001000 11000000 00110000 10000100	J - - -	JANE
		- N - -	JANE
		- A N N	(NULL STATE)
		J O N E	JANE
JOHN	01001000 00101000 01100000 00110000	J - - -	JANE
		- O - -	JOHN
		J O N -	JOHN
		A O N N	JOHN
ADAM	11000000 10001000 11000000 01000001	A - - -	(FALSE STATE)
		- D - -	(FALSE STATE)
		- A - -	ADAM
		- D O M	(NULL STATE)
		J O A M	ADAM
MARY	01000001 11000000 00100001 00001001	M - - -	MARY
		- A - -	JANE
		- R - Y	MARY
		G A N Y	MARY
			MARY
GLEN	10000001 01000010 10000100 00110000	G - - -	GLEN
		- - N	GLEN
		G O E -	GLEN
		A L E N	GLEN
		J A E N	(FALSE STATE)

A 32 x 32 BINARY MEMORY MATRIX BOARD*
FABRICATED WITH OFF-THE-SHELF ELECTRONIC COMPONENTS

DEMONSTRATED FEATURES:

- ASSOCIATIVE NATURE, CONTENT ADDRESSSABILITY

- FAULT - TOLERANCE

- FAST RECALL, IN ONE MACHINE CYCLE ($\sim$ 10 μsec)

- SPURIOUS WORD ERROR CORRECTABLE BY MAKING ASYMMETRIC CONNECTIONS

*PROC. AIAA/ACM/NASA/IEEE COMPUTERS IN AEROSPACE V CONFERENCE LONG BEACH, CALIFORNIA; OCTOBER 1985, P. 160.

JPL   POTENTIAL APPLICATIONS
OF NEURAL NETWORKS

I. INFORMATION STORAGE

- MASSIVE ARCHIVAL/INTERACTIVE INFORMATION BANKS
- RAD HARD, HIGH SPEED, PARALLEL MEMORIES FOR SPACEBORNE COMPUTERS
- INTERACTIVE KNOWLEDGE-BASE FOR AI/EXPERT SYSTEMS
- FAULT-TOLERANT, ASSOCIATIVE MEMORIES FOR ROBOTICS

II PATTERN RECOGNITION

- TARGET RECOGNITION
- NEAREST NEIGHBOR CLASSIFICATION
- VOICE RECOGNITION
- OBJECT (SHAPE), FINGERPRINT (FEATURE) RECOGNITION
- LANGUAGE INTERPRETATION/TRANSLATION
- IMAGE PROCESSING

III COMPUTATION

- ERROR CORRECTION DECODING (COMMUNICATIONS: SPACE, DEFENSE)
- PROCESS OPTIMIZATION AND CONTROL (ROBOTICS, LOGIC MODULES)
- DIRECT INFERENCE AND GENERALIZATION (HARDWARE-BASED EXPERT SYSTEMS)
- SELF ORGANIZATION

JPL

SOFTWARE SIMULATION

INFORMATION STORAGE CAPACITY
OF BINARY MEMORY MATRIX

- DILUTE CODING OF VECTORS IS NECESSARY FOR OPTIMAL INFORMATION STORAGE

  i.e. $M \sim \log_2 N$

  M (VECTOR STRENGTH) = NUMBER OF 'ONES' IN A BINARY VECTOR

- INFORMATION STORAGE CAPACITY:

  I = NO. OF VECTORS STORED x INFORMATION CONTENT PER VECTOR

  $= R \times \log_2 \binom{N}{M}$

  $= R\, M \log_2 N \quad \text{FOR} \quad N \gg M$

STORAGE CAPACITY OF "SMALL" MATRICES

N	M	I_W (bits)	R	I_T (kilobits)	$\bar{\epsilon}_W$ (%)
1024	10	81	3,300	267	<1
	20	142	1,800	255	1
256	8	48	340	16	2
	16	82	200	16	12

N = MATRIX SIZE

M = VECTOR STRENGTH

I_W = INFORMATION CONTENT PER WORD

R = NUMBER OF VECTORS STORED

I_T = TOTAL INFORMATION STORED

$\bar{\epsilon}_W$ = MEAN WORD ERRORS

JPL

CASCADABLE, PROGRAMMABLE, 32 × 32
BINARY MATRIX MEMORY VLSI CHIP
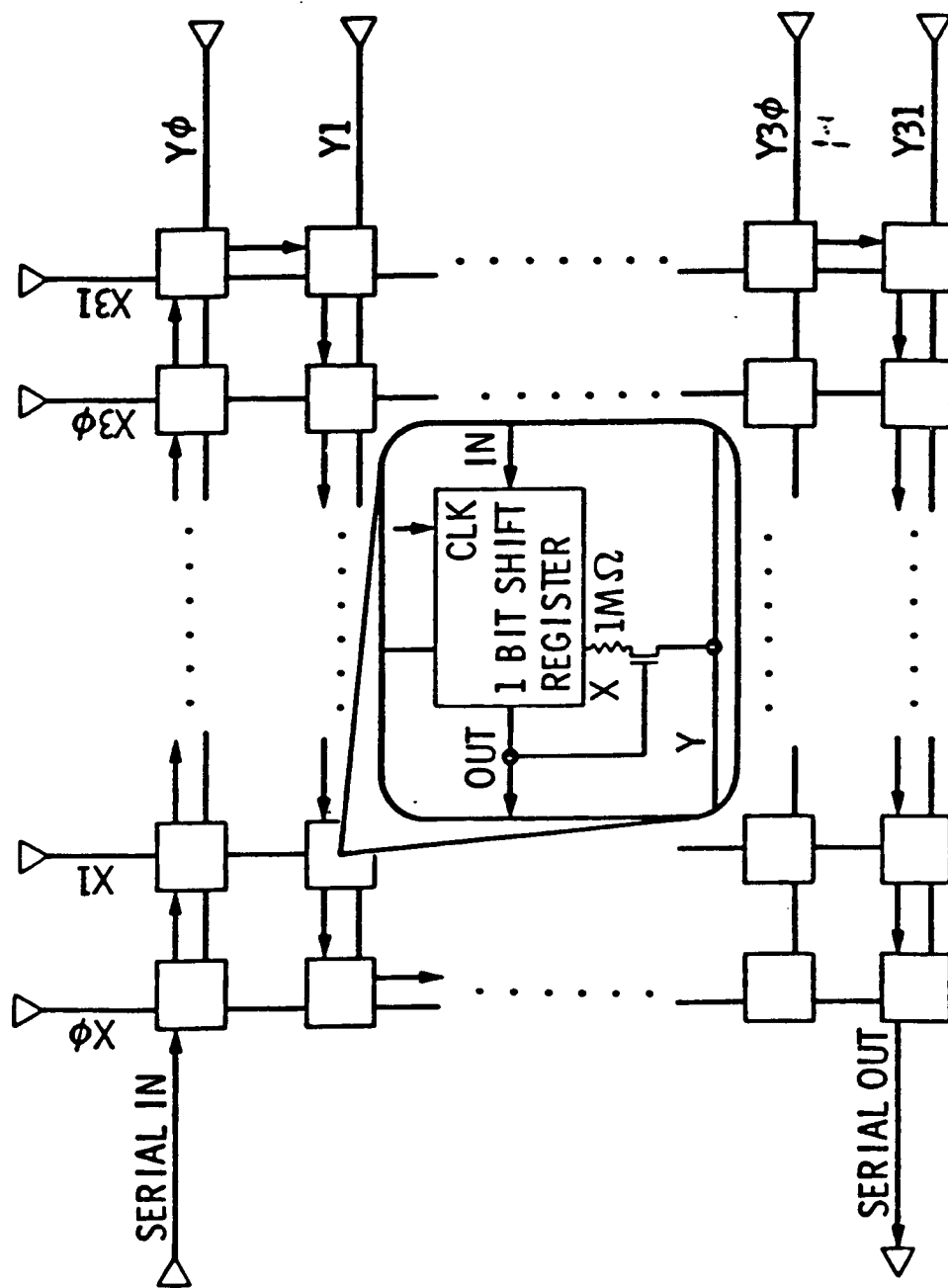
(SCHEMATIC LAYOUT)

WHY THIN FILM MEMORY MATRIX?

- INFORMATION STORAGE IN AN ARRAY OF SIMPLE, TWO TERMINAL, PASSIVE INTERCONNECTIONS IN THIN FILM FORM PROMISES:

  - • HIGH STORAGE DENSITY ($\sim 10^9$ bits/cm^2)

  - • NON-VOLATILITY

  - • MORE INFORMATION PER ACTIVE DEVICE (10^2 TO 10^4 bits/neuron)

  - • POSSIBLE SHARING OF ACTIVE ELECTRONICS (ARRAY OF NEURONS) TO 'ADDRESS' A CHOSEN MEMORY 'BLOCK'

JPL

ULTRA HIGH DENSITY, NON VOLATILE
INFORMATION STORAGE

- ULTRA HIGH   : MEMORY MATRIX   IN THIN FILM FORM
  DENSITY

- NON-VOLATILITY : INTERCONNECTIONS   STABLE MICROSWITCHES
                                         WITH MEMORY

- CONVENIENT   : WRITE/READ/ERASE   SWITCHING
  INPUT/OUTPUT   MECHANISMS?

⇒ TWO TERMINAL, PASSIVE, MEMORY ELEMENT
  AT EACH NODE

UNIQUE FEATURES OF
NEURAL NETWORK MEMORY

JPL

- **ULTRA HIGH DENSITY:** $\sim 10^9$ BITS/CM^2

- **ELECTRONIC INPUT/OUTPUT:** NO MOVING PARTS

- **MEMORY NON-VOLATILE:** RADIATION RESISTANT

- **MEMORY DISTRIBUTED IN 'PASSIVE' INTERCONNECTIONS (SYNAPSES):**
  : LARGE STORAGE CAPACITY (10^2-10^4 BITS) PER ACTIVE DEVICE, (TRANSISTOR)

- **ASSOCIATIVE NATURE:**

- **CONTENT ADDRESSABILITY:** RETRIEVAL FROM PARTIAL INPUT

- **FAULT-TOLERANCE:** RETRIEVAL FROM PARTIALLY INCORRECT INPUT:
  : ALSO, NO LOSS OF INFORMATION BY LOSS OF SOME CONNECTIONS

THE SIMPLEST THIN FILM MATRIX STRUCTURE

SYNAPTIC CONNECTIONS IN SANDWICH GEOMETRY

CONNECTION MATERIAL

METAL

SUBSTRATE
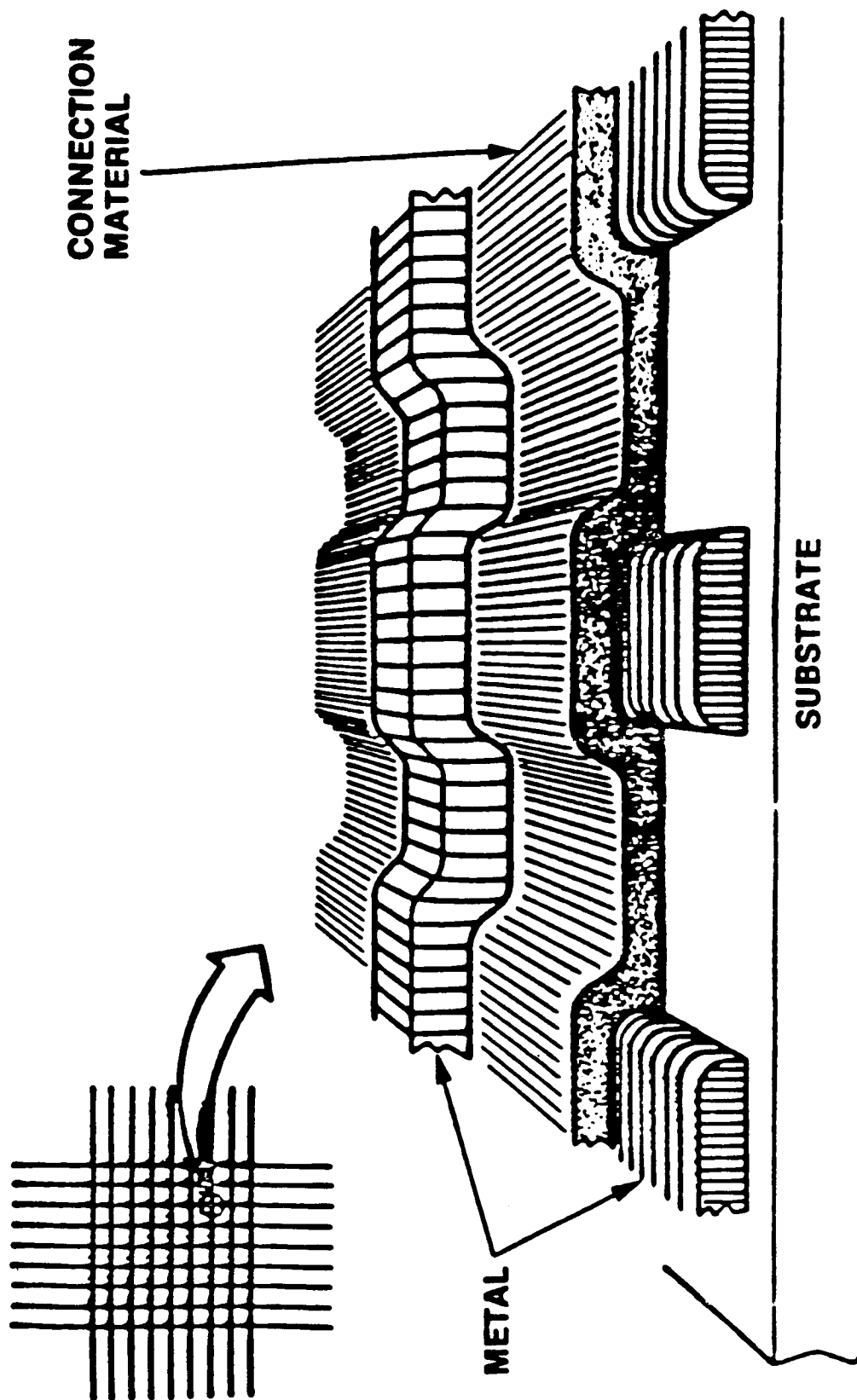
MEMORY SWITCHING IN a-Si:H

MATERIAL EVALUATION

TEST CIRCUIT

PULSE GENERATOR

VOLTAGE

CURRENT

$10^6 \Omega$

a-Si:H

CONDUCTING LAYER

INDIUM TIN OXIDE

SUBSTRATE

RESISTIVITY: $10^7 \Omega$ cm

FILAMENT RESISTANCE

OFF STATE $\sim 2 \times 10^{10} \Omega$

ON STATE $\sim 2 \times 10^5 \Omega$

CONTACT AREA: 1 μm^2 (ESTIMATED)

OFF STATE

ON STATE

ITO: CONDUCTING LAYER

GLASS SUBSTRATE

$\sim 1 \mu m$

0.2 μm

0.1 μm
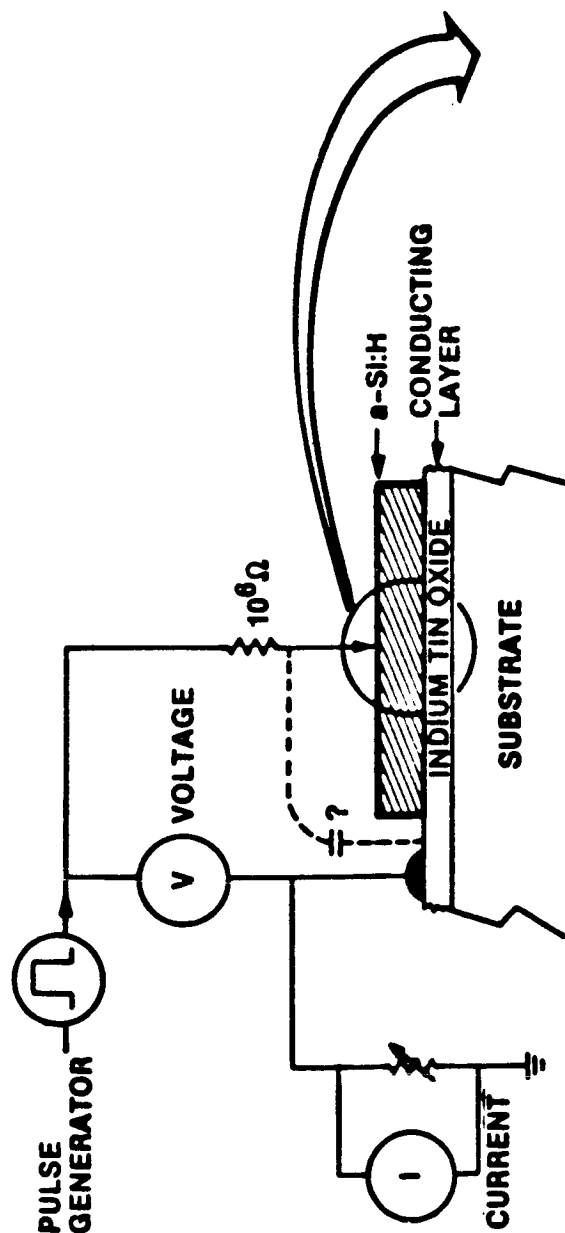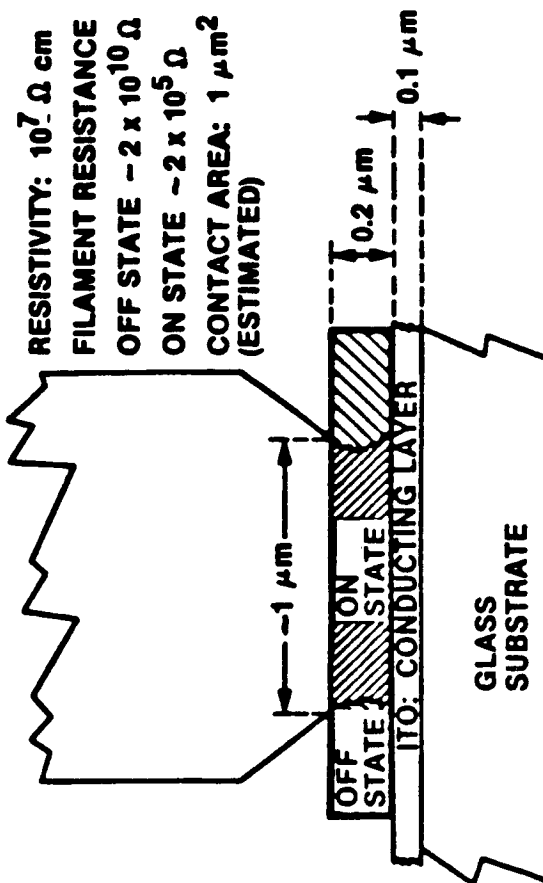
MEMORY SWITCHING IN a–Si:H

I-V CHARACTERISTIC

WITH A BALLAST

RESISTOR (10^6 Ω)

IN SERIES

a-Si-H

E_B 1.5×10^6 V/cm

CURRENT (μA)

VOLTAGE (V)

SANDWICH GEOMETRY

Ni

a-Si:H

Cr

10 μm
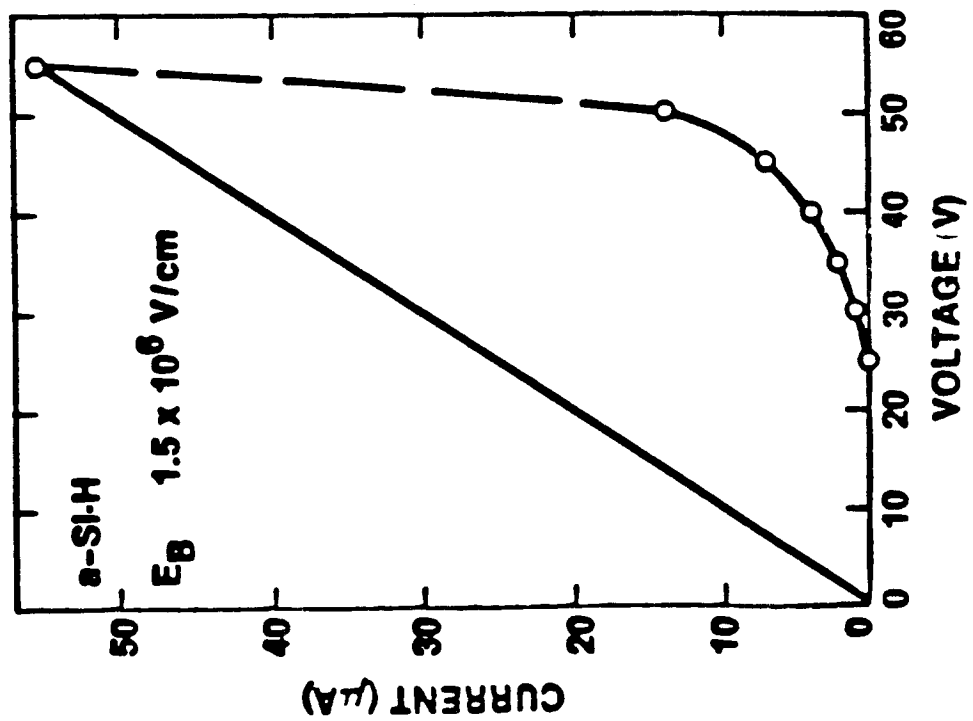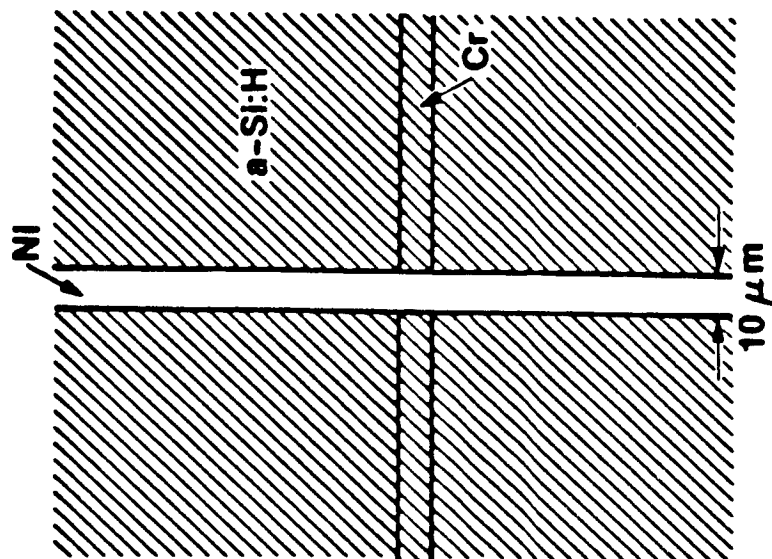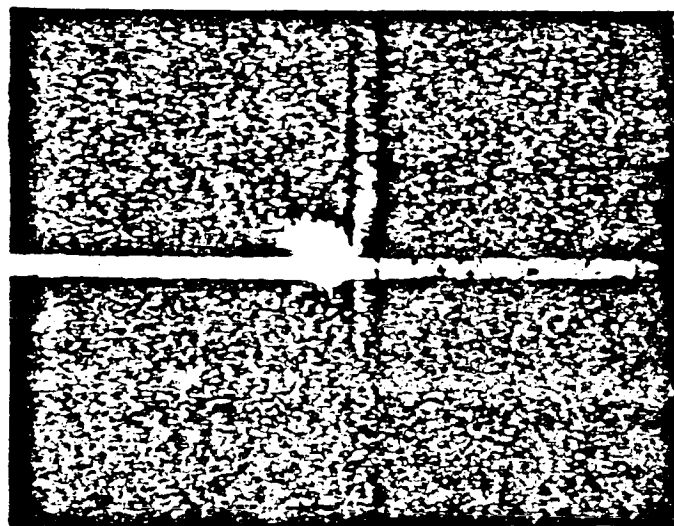
ADVANTAGES:
- SIMPLEST STRUCTURE
- HIGH DENSITY
- $R_{OFF} \sim 10^8 \, \Omega$, $R_{ON} \sim 10^3 \, \Omega$

DISADVANTAGE:
- INCORPORATION OF A STABLE BALLAST RESISTOR DIFFICULT

PLANAR CONFIGURATION

Cr

a-Ge:Aℓ RESISTOR

NI

POLYIMIDE

a-Si:H SWITCHING

a-Si:H

10 μm

R = 8 x 10⁵
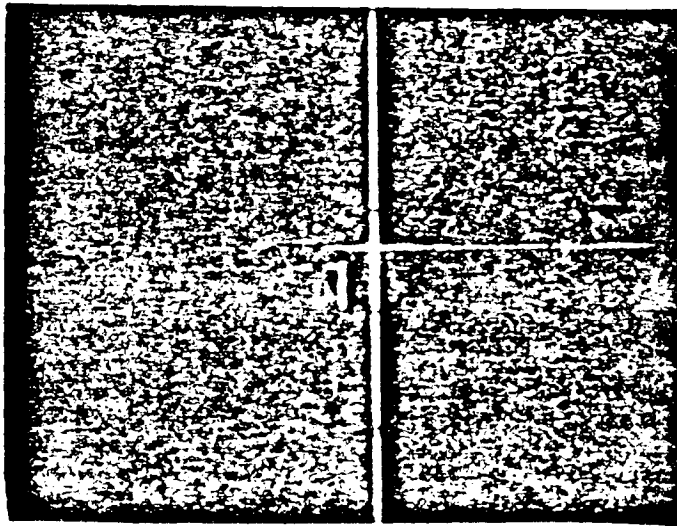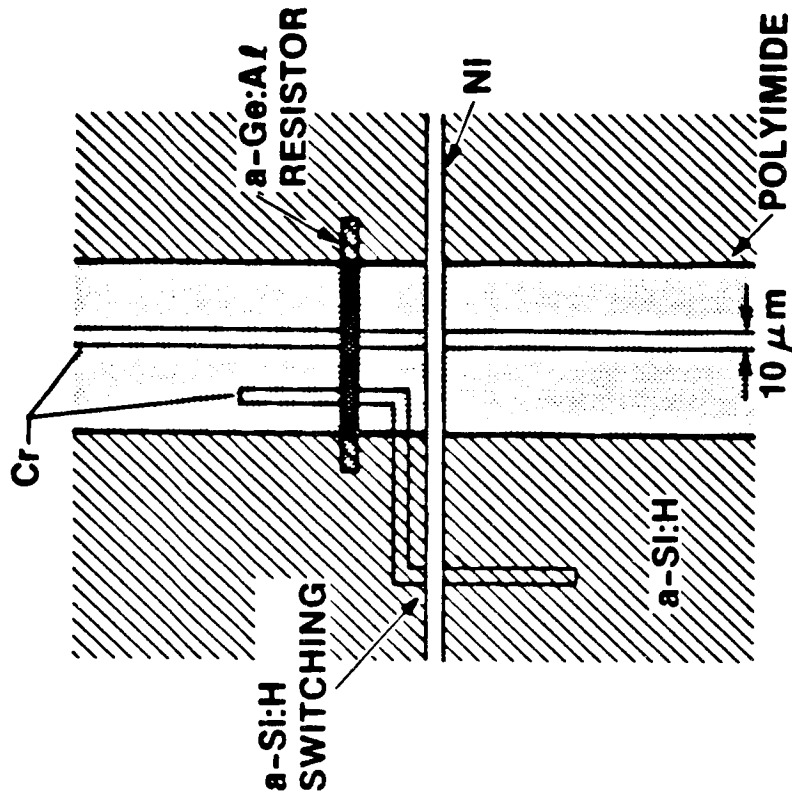
ADVANTAGES:

- BALLAST RESISTOR: a-Ge:Aℓ
  RESISTIVITY TAILORED: 4Ω cm
  LENGTH   = 20 μm
  BREADTH = 10 μm $R = 8 \times 10^5$
  THICKNESS = 1000 Å

- $R_{OFF} \sim 10^8 \, \Omega, \, R_{ON} \sim 8 \times 10^5 \, \Omega$

DISADVANTAGE:

- LOW DENSITY

2-304

SIDE SADDLE STRUCTURE

CROSS SECTIONAL VIEW
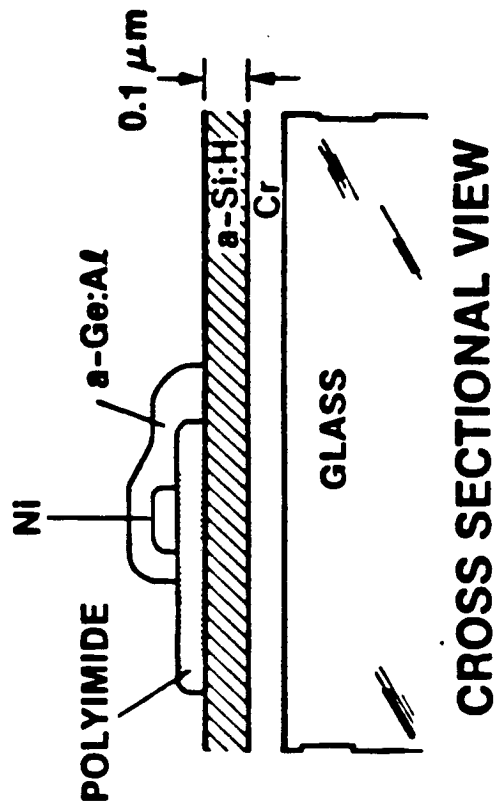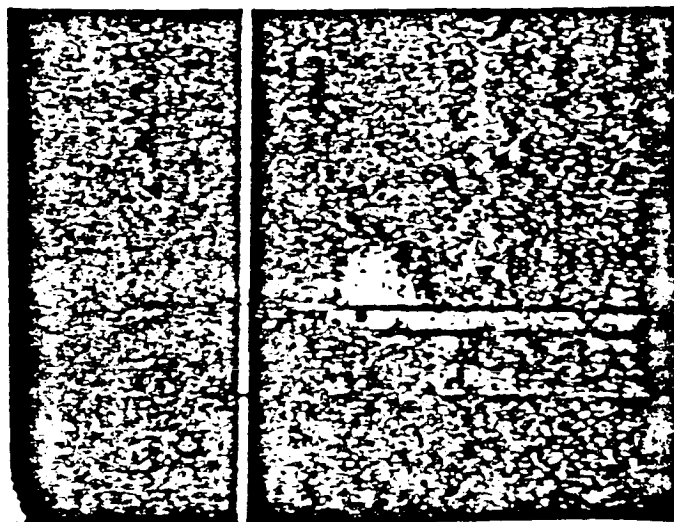
BALLAST RESISTOR OF A SUITABLY TAILORED MATERIAL
IN A VERTICAL OR SIDE-SADDLE GEOMETRY PROMISES
EPROM WITH

- VERY HIGH CONNECTION DENSITY

- CONTROLLED 'ON' RESISTANCE
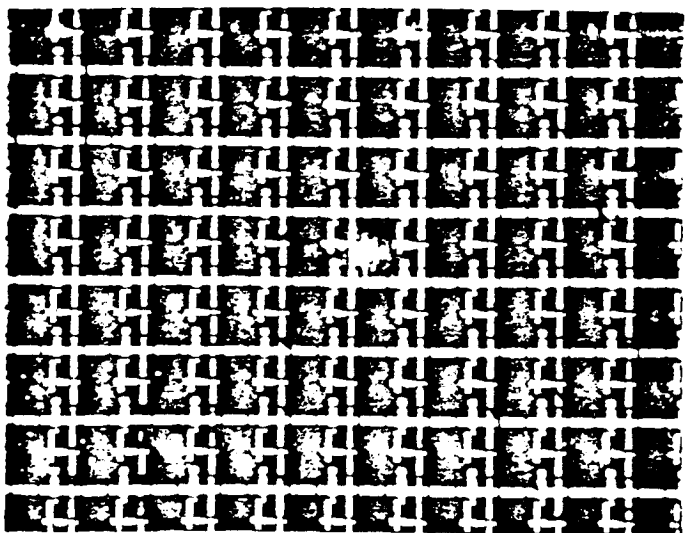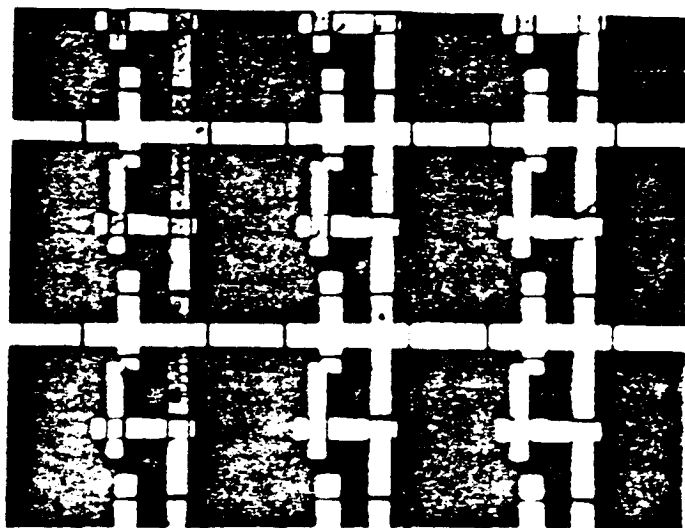
CONCLUSIONS

- BINARY SYNAPTIC CONNECTIONS FABRICATED WITH a-Si:H AS THE SWITCHING MATERIAL AND a-Ge:Aℓ AS THE BALLAST RESISTANCE MATERIAL HAVE SHOWN MEMORY SWITCHING WITH LOW SWITCHING ENERGY

  e.g. 10 μm x 10 μm AREA . . . . ~ 25 nanojoules

  1 μm x 1 μm AREA . . . . ≲ 1 nanojoules

- EPROM BASED ON THE MEMORY SWITCHING IN THE SIDE SADDLE CONFIGURATION AND SUBMICRON LINEWIDTHS MAY APPROACH A DENSITY OF ~ 10^9 CONNECTIONS/cm^2

ELECTRONIC NEURAL NETWORK

- SIMULATION
  - SOFTWARE
  - DISCRETE COMPONENT HARDWARE
  - ANALOG-DIGITAL HYBRID COMPUTER
  - PROGRAMMABLE CASCADABLE CHIP

- DEVICE DEVELOPMENT
  - THIN FILM MEMORY SWITCH WITH BALLAST RESISTOR
  - VLSI NEURON
  - THIN FILM BINARY NEURAL NETWORK
  - ARCHITECTURE FOR BLOCK ADDRESSING
  - WAFER LEVEL INTEGRATION

JPL

ELECTRONIC NEURAL NETWORKS
HARDWARE DEVELOPMENT

- **ROM:** SYNAPTIC CONNECTIONS MADE DURING THE MATRIX FABRICATION PROCESS

    - ULTRA-HIGH DENSITY ASSOCIATIVE MEMORY
    - FAULT TOLERANT PATTERN RECOGNITION

- **PROM:** PROGRAMMABLE BUT NON-ERASABLE SYNAPSES

    - SMART KNOWLEDGE BASE
    - INTELLIGENT INFORMATION PROCESSING

- **EPROM:** ERASABLE, PROGRAMMABLE SYNAPTIC CONNECTIONS

    - LANGUAGE COMPREHENSION
    - COMBINATORIAL OPTIMIZATION
    - AUTONOMOUS LOGIC AND CONTROL OPERATIONS

JPL

OBJECTIVE

TO EXPAND THE INTELLIGENT INFORMATION PROCESSING ABILITIES OF ELECTRONIC NEURAL NETWORKS BY RESEARCH AND DEVELOPMENT OF DEVICE CONFIGURATIONS FOR ERASABLE, NONVOLATILE, THIN FILM MICROSWITCHES (SYNAPSES) FOR ASSOCIATIVE EEPROM
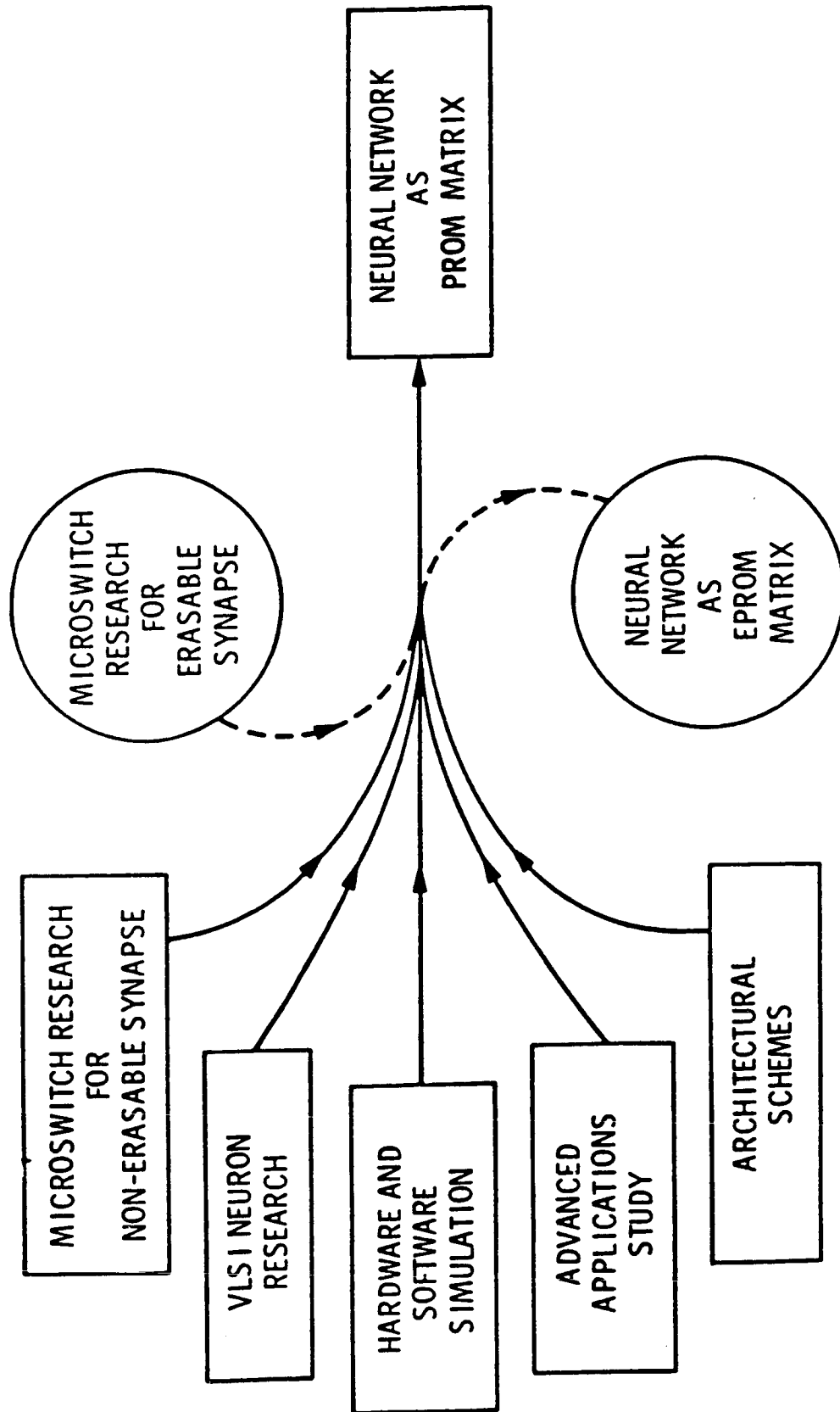
ERASABLE, ELECTRONIC MEMORY SWITCHING

JPL

- SILICON-BASED DEVICES

    FLOATING GATE FET

- AMORPHOUS CHALCOGENIDES

    REVERSIBLE PHASE TRANSFORMATIONS

- NOVEL DEVICE STRUCTURES

    p-n-i JUNCTIONS IN AMORPHOUS SILICON

- ELECTROCHEMICAL SWITCHING

    ELECTROCHROMIC MATERIALS

SYNAPTIC INTERCONNECTS
CANDIDATE MATERIALS

- AMORPHOUS SEMICONDUCTORS

- AMORPHOUS SEMICONDUCTORS ALLOYED WITH METALS

- METAL/DIELECTRIC CERMET SYSTEMS

- TAILORED OXIDES AND NITRIDES

- SILICIDES

JPL

ERASABLE, NON-VOLATILE SYNAPTIC CONNECTORS

- SURVEY OF POTENTIAL CANDIDATES

  NOVEL MATERIALS AND DEVICE STRUCTURES

  FOR THIN FILM MICROSWITCH WITH

  MEMORY AND HIGH PRECISION BALLAST

  RESISTORS

- ARCHITECTURE FOR SYNAPTIC ARRAY

- INTERFACING WITH NEURON ARRAY

- DEVELOPMENT OF NEURAL NET BLOCKS

- SYSTEM INTEGRATION

JPL

ELECTRONIC NEURAL NETWORKS FOR PATTERN RECOGNITION

NEAR-TERM APPLICATIONS

- AUTOMATION AND ROBOTICS

- PERCEPTION AND CONTROL

FOR EXAMPLE:

- TRACKING OF A SPINNING SATELLITE

JPL

SUMMARY

- HARDWARE SIMULATION HAS DEMONSTRATED

  - CIRCUIT STABILITY

  - ASSOCIATIVE NATURE

  - FAULT TOLERANCE

  - FAST RECALL CAPABILITY

  - 100 BITS OF INFORMATION (PARALLEL) READOUT IN 1 μSEC FROM A 1024 x 1024 MATRIX RESULTS IN 10^8 BITS/SEC DATARATE

- BINARY MEMORY MATRICES EXHIBIT SIGNIFICANT INFORMATION STORAGE CAPACITY WITH VIRTUALLY NO ERRORS

  - A 1024 x 1024 MATRIX HOLDS 256K BITS OF INFORMATION

- NON-VOLATILE, THIN FILM CONTENT-ADDRESSABLE MEMORIES BASED ON NEURAL NETWORK CONCEPTS ARE EXPECTED TO REACH HIGH DENSITY

  - SUBMICRON LINEWIDTH SUGGESTS ~10^9 BITS/CM^2

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NASA Computer Science
Research Program Plan Update
1987

Michael McGreevy
Program Manager
Aeronautical Computer Science, CASIS, and Aerospace Human Factors

OAST Computer Science/Data Systems Technical Symposium
Williamsburg, VA
November 20, 1986

1983 Computer Science Research Program Plan
(NASA TM 85631)

● The 1983 plan continues to be a solid foundation.

● goal:

provide technical foundation within NASA to exploit
advancing computing technology in aerospace applications.

● approach:

☐ develop in-house capability in disciplines critical to NASA
☐ conduct focussed research and experimentation
☐ maintain strong university base of fundamental research
   in aerospace computer science

● objectives:

☐ develop advanced aerospace computing concepts
☐ provide theoretical and technology base
☐ strong NASA capability in advanced computer science
☐ support NASA's unique requirements

1983 Computer Science Research Program Plan

● 1983 basis:
  □ NASA's computing requirements and challenges
  □ the state of the art of relevant computer science

● The three themes of the 1983 plan:

  □ Concurrent processing

    system architectures, languages, and algorithms for
    computationally intensive aerospace research problems
    (eg. CFD, image processing)

  □ Highly reliable cost-effective computing

    fault-tolerant architectures; tools and techniques for developing
    verifiably correct software for long-duration unattended
    space missions and man-rated aeronautic and space flight vehicles

  □ Scientific and engineering information management

    effective management and distribution of data to support
    productive agency research, development, and management

1987 Computer Science Research Program Plan Update

● 1987 basis:

    □ NASA's requirements and challenges have evolved

    □ the state of the art has clearly advanced

● The original themes continue to be valid, though "reliability" and "effective distribution of data" have gained new meaning, and new parallel systems are available (e.g Connection Machine).

● New themes are emerging:

    □ **Software engineering**

        e.g. the challenge of Space Station software;
            ADA; lifecycle management...

    □ **Artificial Intelligence**

        e.g. knowledge acquisition; learning; reasoning under uncertainty; verification of expert systems...

1987 Computer Science Research Program Plan Update

- Our approach to the original themes may need to be updated.

  For example:

  ☐ Is NASA conducting Concurrent Processing research in a focussed and coordinated way which addresses the the Agency's unique requirements?

  ☐ Is NASA effectively using its computer science expertise to handle the technical information glut?

  ☐ Are the Agency's unique requirements for communication of mission critical scientific, engineering, and management information being met?

  ☐ Can NASA remain capable in advanced computer science with its current funding and personnel strategies?

1983 Computer Science Research Program Plan

- 1983 NASA Program Overview:

  □ Design and analysis methods

  □ Simulator systems

  □ Handling of experimental data

  □ Flight crucial systems

  □ Operations

  □ Computational modeling of physical processes

  □ Management applications

  □ Engineering applications

- Q: In what areas can NASA's computer science expertise make critical contributions to the missions of the Agency?

1987 Computer Science Research Program Plan Update

- Milestones:

  □ November 1986: kickoff plan update activity;

  □ December 1986: form intercenter plan update committee;

  □ January-March 1987: draft new plan in expanded PASO format, and establish mechanism for in-house peer review;

  □ June 1987: peer review of in-house computer science program, and consideration of new studies;

  □ July 1987: selected studies form basis of RTOP negotiation;

  □ August 1987: Software Engineering Symposium, and begin to build advocacy for FY89 augmentation;

  □ September 1987: rewrite of 1983 Computer Science Research Program Plan Technical Memorandum

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PASO: Plans and Specific Objectives
RTOP: Research and Technology Operating Plan

CLOSING REMARKS

The afternoon session on Thursday, November 20, was devoted to a CSTI Planning Session that was led by Richard Grumm (JPL) and John Dalton (GSFC). As a result of this effort, a Data Systems Technology Working Group was organized as part of the CSTI Initiative.* The makeup of the DSTW Group is as follows:

Chairman — R. Kreider, OAST/HQ
Members — H. Benz, LaRC
          T. Grant, ARC
          D. Nichols, JPL
          J. Dalton, GSFC

Members representing JSC, MSFC and LeRC are to be named at a later date.

The third Computer Sciences and Data Systems Technical Symposium adjourned following the conclusion of the DSTW planning session. The fourth gathering is tentatively scheduled to be held at ARC in the Spring of 1988.

*A parallel working group concerned with Computer Sciences was organized during an ad hoc evening session held on November 18. The Computer Sciences Working Group is headed by Mike McGreevy (OAST/HQ) and Sue Voigt (LaRC).

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15. Supplementary Notes

16. Abstract

Presentations of OAST-supported work in progress were made by NASA personnel from Centers, Institutes, and Universities. The Computer Sciences subject material was grouped into the following categories: Software Engineering, University Grants, Institutes and Applications. The material presented under Data Systems was not categorized, as such. The Symposium was held at the National Conference Center in Williamsburg, Virginia from November 18 to 20, 1986. The Symposium schedule and the list of attendees are included.

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